

TOSHIBA MOS MEMORY PRODUCTS

256 WORD x 4 BIT CMOS RAM

TC5501P/-I
TC5501D/-I

DESCRIPTION

The TC5501P/D is a fully static read write memory organized as 256 words by 4 bits using CMOS technology. Because of ultra low power dissipation, the TC5501P/D can be used as battery operated portable memory system and also as a nonvolatile memory with battery back up. The TC5501P/D operates from a single 5V power supply with a static operation, so that the no refresh periods are required. This simplifies the power supply circuit design.

The three state outputs simplify the memory expansion making the TC5501P/D suitable for use in a microprocessor peripheral memory. Since the minimum data retention voltage is 2V, the battery back up system needs only simple circuit. By using Toshiba's original C²MOS technology, the device circuitry is not only simplified but wide operating margin and noise margin are also realized.

The TC5501P/D is offered in standard 22 pin plastic and cerdip packages, 0.4 inch in width.

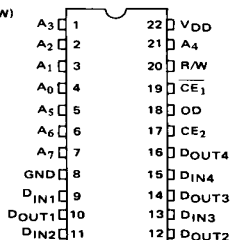
FEATURES

- Low Power Dissipation
 - 55μW (MAX.) STANDBY
 - 83mW (MAX.) OPERATING
- Single 5V Power Supply
- Data Retention Voltage 2V to 5.5V
- Package
 - Plastic DIP : TC5501P
 - Cerdip DIP : TC5501D

- Fully static operation
- Three State Output
- Input/output, TTL Compatible
- Access Time
 - TC5501P/D ; $t_{ACC} \leq 450\text{ns (MAX.)}$
 - TC5501P-1/D-1; $t_{ACC} \leq 650\text{ns (MAX.)}$

PIN CONNECTION

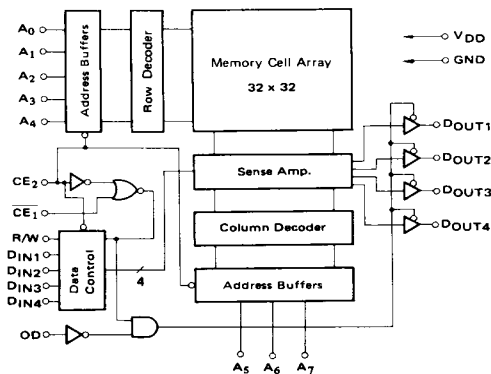
(TOP VIEW)



PIN NAMES

A ₀ ~ A ₇	Address Inputs
R/W	Read Write Input
CE ₁ , CE ₂	Chip Enable Inputs
DIN ₁ ~ 4	Data Inputs
DOUT ₁ ~ 4	Data Outputs
OD	Output Disable Input
V _{DD} /GND	Power Supply Terminals

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3 ~ V _{DD} + 0.3	V
V _{OUT}	Output Voltage	0 ~ V _{DD}	V
P _D	Power Dissipation (T _a = 85°C)	800	mW
T _{SOLDER}	Soldering Temperature - Time	260 · 10	°C · sec
T _{STG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	-30 ~ 85	°C

DC RECOMMENDED OPERATING CONDITION

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V _{DD}	Power Supply Voltage	4.5	—	5.5	V
V _{IH}	Input High Level Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Level Voltage	-0.3	—	0.65	V
V _{DH}	Data Retention Voltage	2.0	—	5.5	V

DC CHARACTERISTICS (T_a = -30 ~ 85°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
I _{IN}	Input Current	0 ≤ V _{IN} ≤ V _{DD}	—	±0.05	±1.0	μA
I _{DDS}	Standby Current	V _{DD} = 2.0V to 5.5V CE ₂ = 0.2V, Output open	—	0.2	10	μA
I _{DDO}	Operating Current	V _{DD} = 5.5V, t _{CYC} = 1μs	—	6.2	15	mA
I _{LO}	Output Leakage Current	0 ≤ V _{OUT} ≤ V _{DD}	—	±0.05	±1.0	μA
I _{OH}	Output High Current	V _{DD} = 4.5V, V _{OH} = 2.4V	-1.0	-2.0	—	mA
I _{OL}	Output Low Current	V _{DD} = 4.5V, V _{OL} = 0.4V	2.0	3.0	—	mA

Note (1) T_a = 25°C V_{DD} = 5V

CAPACITANCE (2) (T_a = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V, f = 1MHz	—	5	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V, f = 1MHz	—	7	15	pF

Note (2) This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

● READ CYCLE

SYMBOL	PARAMETER	TC5501P/D		TC5501P-1/D-1		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	450	—	650	—	ns
t _{ACC}	Address Access Time	—	450	—	650	ns
t _{ACC1}	CE ₁ Access Time	—	400	—	600	ns
t _{ACC2}	CE ₂ Access Time	—	500	—	700	ns
t _{OD0}	OD Access Time	—	250	—	350	ns
t _{COE}	Output Enable Time	0	—	0	—	ns
t _{DIS}	Output Disable Time	0	130	0	150	ns
t _{OH}	Output Data Hold Time	0	—	0	—	ns

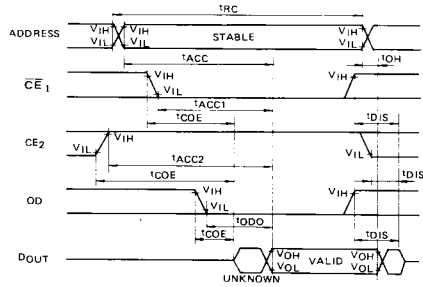
● WRITE CYCLE

SYMBOL	PARAMETER	TC5501P/D		TC5501P-1/D-1		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	450	—	650	—	ns
t _{AW}	Address Setup Time	130	—	150	—	ns
t _{CW}	CE ₂ Setup Time	130	—	150	—	ns
t _{WP}	Write Pulse Width	250	—	400	—	ns
t _{DS}	Data Setup Time	250	—	400	—	ns
t _{DH}	Data Hold Time	50	—	100	—	ns
t _{WR}	Write Recovery Time	50	—	50	—	ns

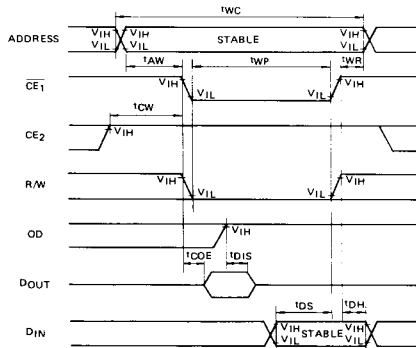
A.C. TEST CONDITIONS

- Output Load : 100 pF + 1 TTL Gate
- Input Pulse Levels : 0.45V, 2.4V
- Timing Measurement Reference Levels
 - Input : 0.65V, 2.2V
 - Output : 0.65V, 2.2V
- Input Pulse Rise and Fall Times : 10ns

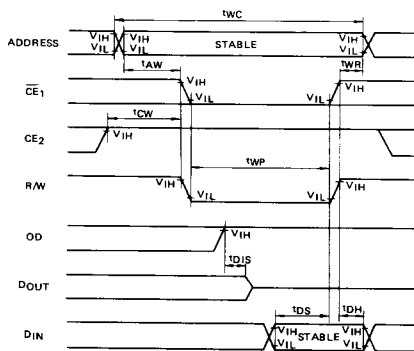
Read Cycle



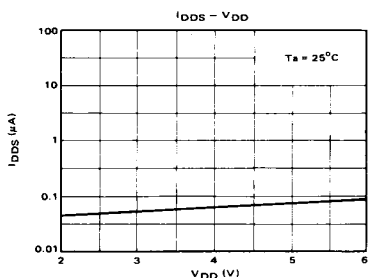
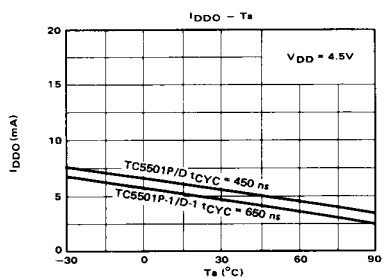
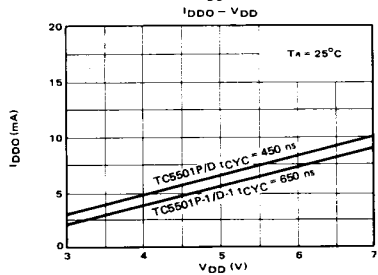
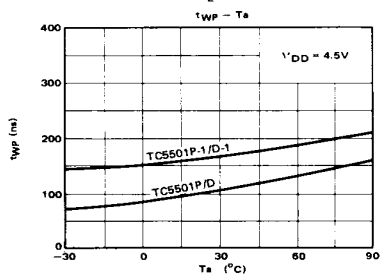
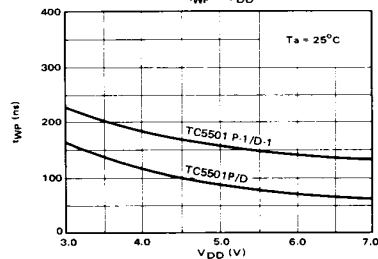
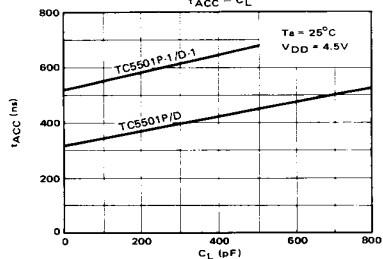
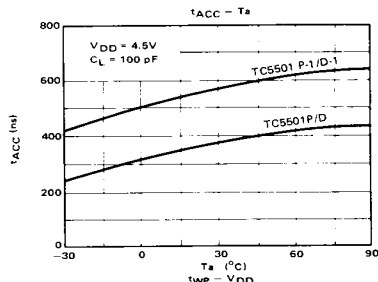
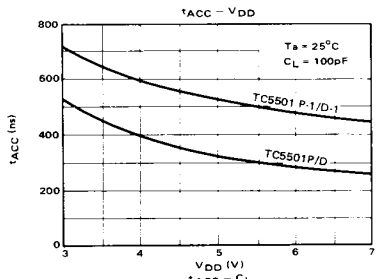
Write Cycle 1

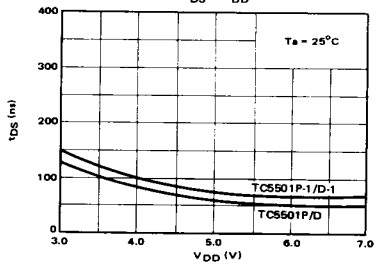
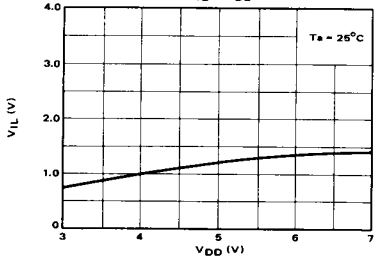
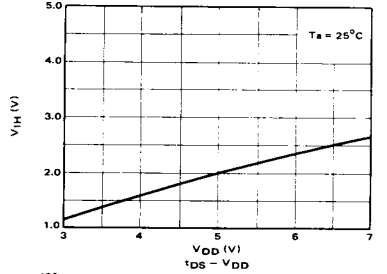
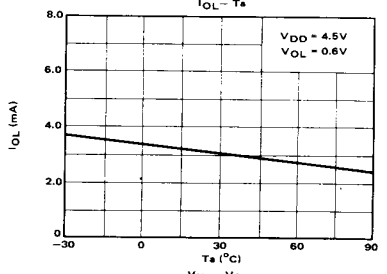
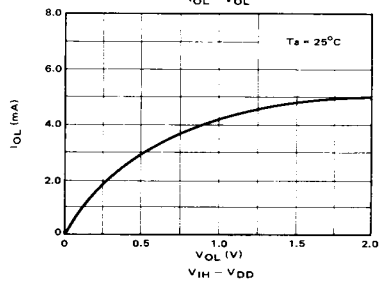
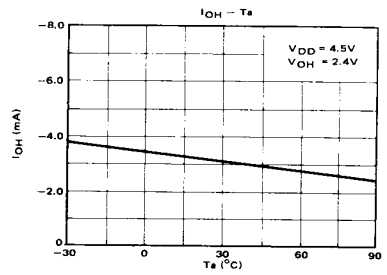
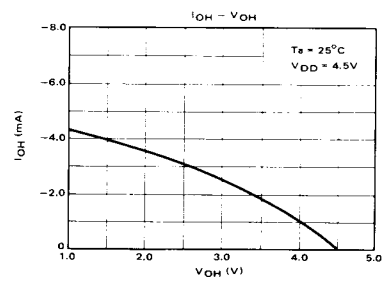
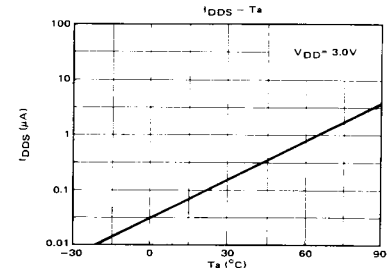


Write Cycle 2

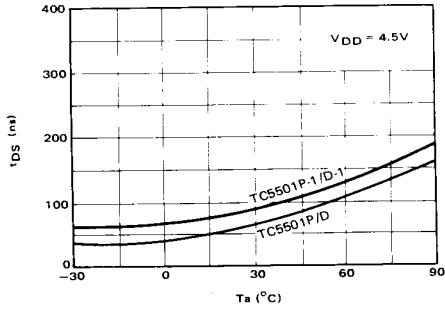


TYPICAL CHARACTERISTICS

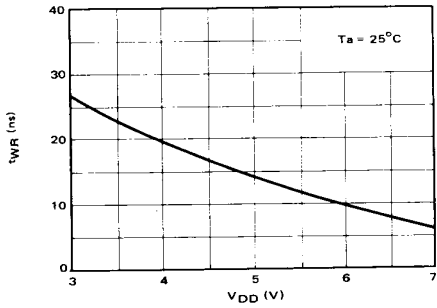




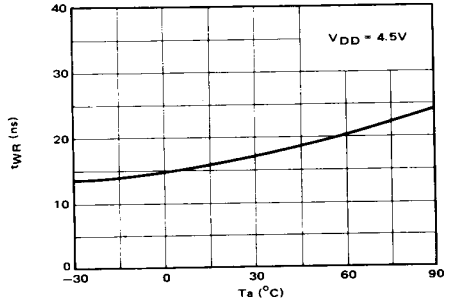
$t_{DS} - T_a$



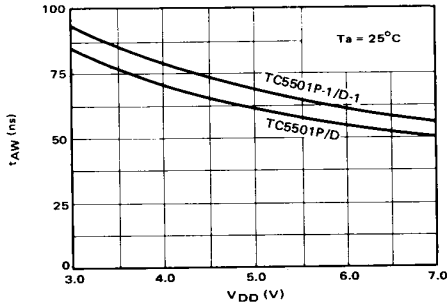
$t_{WR} - V_{DD}$



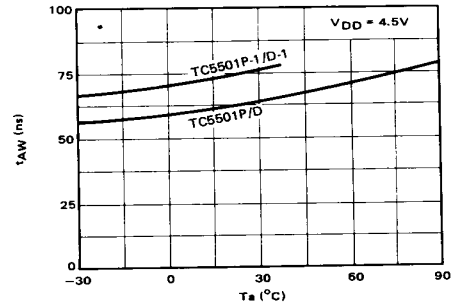
$t_{WR} - T_a$



$t_{AW} - V_{DD}$

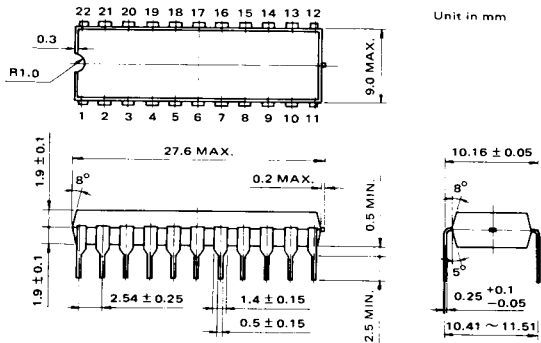


$t_{AW} - T_a$

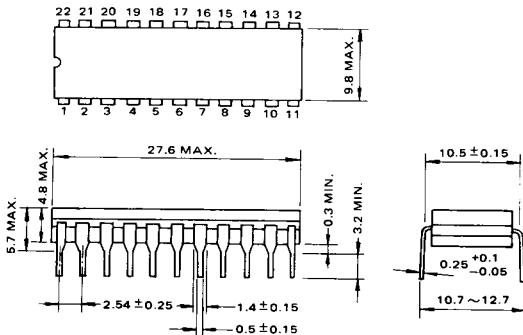


OUTLINE DRAWINGS

PLASTIC PACKAGE



CERDIP PACKAGE



Notes: Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 22 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.
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