Field Engineering Manual

System 8870

Models 2, 4, and 6

Summary of I/O Card Assignments

4.79

1st Edition

Order Number: S 0445 101 04 79





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8870/2/4/6

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interrupt Release While Operating the

Index of abbreviations

AG	output
AWD	automatic dialling unit
BLZ	block length counter
DTEA	display-keyboard I/O unit
DÜST	communications control unit
EG	input ************************************
FB	busy flip-flop
GA	device address
KAR	head address register
KE	coupling unit
LKS	card punch
LMVG	read and compare
LSL	paper tape reader
LSS	paper tape punch
LVG	read and compare
PSP	parallel periphery interface
RAL	random access load
SPD	track difference counter
SS - N 820	interface Níxdorf 820
WT	framing pulse
ZDV	line printer DMA feature

Value of the control of the control



1 1/0 2802

The I/O is used as an interface converter from the SS 901 to the SS 820 and the PSP.

1.1 I/O Assignment

Address of the coupling unit
 Address of peripheral equipment on the SSN 820 and the PSP

100, 10 of this document and giving it is 31 is a set of communication follows for communication of the form of the communication of the grant of a pair it is model or design to fail it is model to design.

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1.1.1 Description of I/O Assignment

There are 4 input and 3 output instructions.

1.1.1.1 Input Instructions

- EG 0.0.0 Interrupt interrogation instruction
- EG X.0.0 Interrogation instruction for the interrupt register of the coupling unit.
- EG X.O.1 Interrogate status bits
 - Bit 1 The SS-N820 has signalled a power failure.
 - Bit 2 Time fault in the PSP.

A time fault is present if there is no acknowledge signal within 2.4 us after "start information" is outputted.

Bits 1 and 2 can be outputted in combination.

- Bit 3 Parity error in the PSP.
- EG X.Y.Y Input instruction for peripheral equipment.

1.1.1.2 Output Instructions

- AG X.0.0 Output the interrupt number, the interrupt disable or interrupt enable and the interrupt priority definition.
 - Bit 12 Bit 12 = "0"
 Interrupt number is outputted in bits 1 to 8.

Bit 12 = "1" and bit 1 = "0"

The interrupt disable is cancelled.

Bit 12 = "1" and bit 1 = "1"The interrupt number disable is implemented.

Bit 12 = "1" and bit 2 = "0"

the interrupt of the SS-N820 has highest priority.

Bit 12 = "1" and bit 2 = "1"

The interrupt of the disk store has highest priority.

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AG N. O. I DETECT STATEMENT	•	AG	X.0.1	Delete	status	bits
-----------------------------	---	----	-------	--------	--------	------

Bit 1 Is used to generate the clear signal on PSP bus 1.

Bit 1 is to be outputted twice, once as "1" (delete is outputted), and once as "0" (delete is cancelled).

Bit 2 Is used to generate the clear signal on PSP bus 2.

Bit 2 is to be outputted twice, once as "1" (delete is outputted), and once as "0" (delete is cancelled).

Bit 3 Is used to generate the clear signal on SS-N820.

Bit 3 is to be outputted twice, once as "1" (delete is outputted), and once as "0" (delete is cancelled). The state of the

- Bit 4 Is used to delete error flags ZF (time error) and PF (parity error).
- AG X.Y.Y Output instruction to operate peripheral device.

1.2 Coupling Unit (KE) 2802 Interrupt Release

The KE does not itself generate interrupt signals i.e. interrupt triggering is by recognition of an interrupt signal from a peripheral device. The interrupt number which is thus generated consists of both the interrupt number of the KE and the interrupt number of the peripheral device.

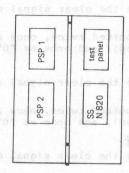
1.3 KE 2802 Addressing

- Address 4.0.0 = Internal I/O instruction and I/O instruction for the SS-N820
- Address 5.0.0 = I/O instruction for SS-N820
- Address 3.0.0 = I/O instruction for PSP bus 1
- Address 7.0.0 = I/O instruction for PSP bus 2



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1.4 Physical Layout



1.5 Test Point Assignment of the 820 Test Panel

Top view of contact side

- Eln Aln Dln
- E2N A2N D2N
- E3N A3N D3N
- E3N A3N D3N
 E4N A4N D4N
- E5N A5N D5N
- ESN ASN DSN
- E6N A6N D6N E7N A7N D7N
- E7N A7N D7N E8N A8N D8N •
- E8N A8N D8N •
- E9N A9N D9N •
- Elln Alln Dlln •
- Elln Alln Dlln El2n Al2n EANFN •
- NAN INSEN EATRN •
- EGN AGN LO •



- Printer Connection to PSP via KE 2802 2
- I/O Assignment of the 4552.xx Printer to the PSP 2.1

DP print error test test type of printer —	DF PF	DF PF print error paper (lint test	interrupt number (alw print error paper error feed active INT test end of feed active interrupt number ————————————————————————————————————	interrupt number (always) DF	interrupt number (alw print error paper error feed active interrupt number (alw print error paper error feed active interrupt number error data for block transmissi errupt number error control character error control character error start print position error error print position error e	Bit Row	EG 0.0	EG Y.0	EG Y.1	EG Y.2	EG Y.3	AG 0.1	AG Y.0	AG Y.1	AG Y.2	AG Y.3	
DF print error int test test printer	6 P F error P F O G P F F F F F F F F F F F F F F F F F F	6 day	interrupt number (alw error paper error feed active and of feed active ac	interrupt number (always) interrupt number (always) interrupt number (always) interrupt number (always) data for block transmission data for block transmission control character control character control character	interrupt number (always) error paper error feed active printer active end of paper and of feed active print and of block and of feed active feed active and of block transmission data for block transmission data for block transmission control character control character control character	80	la i qu	NO 16	v Dae	LNI	type of	i lo i m	1 g - 0	T			
	P P P P P P P P P P P P P P P P P P P	P P P P P P P P P P P P P P P P P P P	interrupt number (alw paper error (feed active and of feed active interrupt number and of feed active and of feed active and of feed active and act for block transmissi and of feed active and act for block transmissi and of feed active and act for block transmissi and active	interrupt number (always) interrupt number (always) pr	interrupt number (always) interrupt number (always) PF ygger error feed active printer active end of paper and of peed active printer active end of block ransmission data for block transmission data for block transmission and of data for block transmission attraction number control character start print position	7		lead s	DF print error	INT	printer	1 7 51 182 11 1 19 3 14	root geg	636 (6 96 (4 96 (4			

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2.1.1 Description of I/O Assignment

There are 5 input and 5 output instructions.

2.1.1.1 Input Instructions

- EG 0.0.0 Interrogate Interrupt number
- Interrogate the interrupt register of the printer control unit
- EG Y.1 Printer status bits
 - Bit 1 KLAR (ready)

This bit is set if the printer is ready to operate.

Note that this bit is only set if:

- a) The printer is switched on,
- b) The drum arm is closed,
- The printer drum has reached its normal running speed,
- d) the punched tape of the channel feed device has been read in, if the latter is switched on,
- e) No print hammer fault,
- f) No ink ribbon fault,
- g) No format fault,
- h) No paper fault,
- i) No incorrect character has been transferred,
- k) The previous paper feed was completed within 2.5 s,
- 1) There is no fault in the punched tape and
- m) A non-punched channel of the feed tape has not been selected.
- Bit 2 DATANF

This bit is set when the printer is ready to accept data.

Bit 3 PAE

This bit is set when end of paper is reached.

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THE RESERVE THE PERSON NAMED IN COLUMN 1		
COMPUTER		8870/2/4/6
Bit 4	End of priot interrupt AD	
	This bit is set when a printing process being carried out.	; is
Bit 5	VR squaresque	
	This bit is set when paper is being fee	i.
Bit 6	PF eldsoliggs 108	
	This bit is set when the following cond are satisfied:	litions
	a) A feed fault has occurred,	
	b) The paper has run out of the tracto	or,
	c) Paper feed has not been completed w	vithin
	d) PAE (end of paper) is set and the I of the form has reached the printir	ng
Bit 7	DE	Y.X GB 6
es character i		or.
	The following conditions entail the set bit 7:	ting of
	An incorrect character has been present processing or there is a print hammer for	ed for ault.
Bit 8	Not applicable	
• EG X.Y.2	Interrogate cause of interrupt	
Bit 1	Delete	
and on the color		
	this bit is set if the printer was swit or if there was a power failure.	ched off,
Bit 2	Parity error	
	this bit is set if a parity error is deduring data transmission in the PSP.	
Bit 3	End of block interrupt	
	this bit is set if the end of block chais detected in the printer during automodata transmission (only in the DMA oper mode).	natic



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Bit 4 End of print interrupt

This bit is set at the end of a printing

process .

Bit 5 Feed interrupt

This bit is set when feed has been completed.

Bit 6 Not applicable

Check interrupt Bit 7

This bit is set when a check interrupt is released.

Bit 8 Interrupt for son basic ason

This bit provides a general indication that an interrupt is present and appears together with

every interrupt.

EG X.Y.3 Interrogate drum and printer type

Drum type

Various types of drums with different character sequences and founts can be used in conjunction with the printer equipment. The table below gives details of available drum types and their respective codes. Coding is by means of inserting the relevant PROM card assigned to each drum type.

Bit						Designation
assignment	5	4	3	2	1	of drum type
dquizada	0	0	0	0	0	ASCII-DP 64-character
	0	0	0	0	1	ASCII-DP 96-character
	0	0		1	0	Standard 64-character 60-character set: OCR-B1
			1	100		

0 0 0 1 1 Standard 96-character 96-character set:

ORC-B1

Printer type

Bits 7 and 8 indicate the type of printer.

assignment	7	6	Line printer
AMG and ni v	1	Onolesiasa	Print speed 300 lines/minute
	î	1	Print speed 600 lines/minute

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2.1.1.2 Output Instructions

- AG 0.1 This is not an output instruction. The AG 0.1 statement relates to automatic data transmission; automatic data transmission is initialized by AG 0.1.
- AG X.Y.O The interrupt number is outputted to the interrupt register of the printer.
- AG X.Y.1 Print data is outputted by the CPU (central processing unit) to the printer direct (no DMA mode).
- AG X.Y.2 Control characters transferred to the printer.

Instruction code	Meaning
0.0	Release interrupt disable
0.1	Delete all flags (general deletion) and implement interrupt disable
0.2	Delete "PSP parity error" and "delete" flags
0.3	Start DMA (set ANFR for auto- matic data transmission)
0.4	Delete "Int. end of block" flag
0.5	Delete "Int. end of print" flag
0.6	Delete "Int. end of feed" flag
0.7	
0.8	Delete "Check interrupt" flag
0.9	Release check interrupt
0.10	
0.11	
0.12	
0.13	release printing
8.0	disable interrupt

AG X.Y.3 Output start print position.

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- - Bit 1 to 7 These bits contain the value for the feed depending on the content of bit 5.

If bit 5 = "1" then bits 1 to 4 and bits 6 and 7 contain the number of line feeds.

If bit 5 = "0" then bits 1 to 4 contain the channel number of the channel feed.

2.2 Interrupt Release

The completion of a printing process is signalled by an interrupt. Any fault conditions are likewise signalled to the system by an interrupt.

2.3 Addressing

Address bits 5 to 8 are used for addressing. Address X.Y.Z

X = KE 2802 of DSZ 1804 address

Y = Printer control address

Z = Line A ANG State



3 1/0 0317.03

The I/O is used to drive the 0611 magnetic tape on the $8870\,\mathrm{m}$ system (recording density $800\,\mathrm{bits}$ per inch).

3.1 I/O Assignment

Row Bit	EG Y.1	EG Y.2	EG Y.4	EG Y.8	EG Y + 2.0	AG Y.1	AG Y.2	AG Y.4	AG Y.8	AG Y + 2.0
12	ane ore	ite to J	iw sq	116 OK	CRC arithmetic unit	e ios	den: de 3.	93. 93. 565:	1W 5W	
ाा	280	bas	pali	haiw	netic unit	do	alb ray	edos	dT 93	
10							935 011	eqe.	to Rei	
6	channel 9	Write	bei	nua.	channel 9	channel 9	10 at	101 103 -	ies MT	
80	channel 8	Rewin -		TOS	channel 8	channel 8	o en	ani)	ron seg	
7	channel 7	Ready	0 361	933	channel 7	channel 7	10 TO	cle	(83 (89	
9	channel 6	Beginning of Tape	0260	bal	channel 6	channel 6	97U31	clear input store	toT toT	Parity ODD (1) EVEN (0)
5	read channel 5	parity and echo error	. Des	toests logs	channel 5	write channel 5	Rewind + Lockout		eria Ere e e e	clear CRC register
4	channel 4	temp. error	ig It	міль.	channel 4	channel 4	Rewind	08 . Ve		read
6	channel 3	End of Tape	buffer empty (read)	SE 87	channel 3		Write Permit	i ed Modi		
2	channel 2	Bit detected	buffer full (write)	MO3	channel 2	channel 3 channel 2	Forw.(1) Rev. (0)	il bi audi		_ e
-	channel 1	Write	end of block detector		channel 1	channel 1	Run (1) Stop (0)			

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3.1.1 Description of I/O Assignment

The following I/O instructions are available in the operating program for the control of the magnetic tape station via the I/O 0317.03.

3.1.1.1 Input Instructions

Bit 1 - 9 Read in character from tape. Status messages

EG Y.2

Bit 1 Write power, i.e. erase and write heads are switched on-

Bit 2

Bit detected

Bit 3

Not evaluated by channel program.

End of tape (EOT)

End of tape mark detected. This message is stored in a flip-flop.

Bit 4

Temperature error

Temperature sensor indicates that permissible tape deck temperature has been exceeded.

Bit 5

Parity or echo error

Not evaluated by channel program.

Bit 6

Beginning of tape (BOT)

Beginning of tape mark detected at photodiode.

Bit 7

Ready

The tape deck is switched to "remote" and ready to operate.

Bit 8

Rewinding

The tape deck is rewinding and has not yet reached BOT.

Bit 9

Write enable

Write is enabled because write enable ring is loaded (write enable contact closed).

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• EG Y.4

Bit 1 Block end message

Not evaluated by channel program.

Bit 2 Buffer full (write)

Message from FIFO, i.e. buffer contains 64 characters.

Bit 3 Buffer empty (read)

The message resets, a write flip-flop and switches over to "read".

EG Y + 2.0 CRC arithmetic unit
 The CRC character formed in the arithmetic unit register is ready.

3.1.1.2 Output Instructions

- AG Y.1

 Bits 1 9 Write Information
- AG Y.2 Control bits

 Run/stop

 1 = Run

 0 = Stop
 - Bit 2 Forward/reverse 1 = Forward 0 = Reverse
 - Bit 3 Write permit (write permit)
 - Bit 4 Rewind

 The tape is wound back to the beginning of tape mark (BOT).
 - Bit 5 Rewind and lock out
 In addition to rewind, the tape is wound past
 BOT, the tape station switches to "reset" and
 the vacuum is switched off.
- AG Y.4 Clear input store

 All status flip-flops and the system are reset.



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AG Y + 2.0

Read enable Bit 4

Specific release of buffer for "read" or "check

read".

Bit 5 Clear CRC register

i.e. null exchange

Parity 1 = ODD parity 0 = EVEN parity

3.2 Interrupt Release

The I/O 0317.03 cannot be interrupted and is controlled via the clock interrupt.

33 Addressing

Address bits 5 to 8 are used. Bit 6 has a special function and is used to address the CRC arithmetic unit, the read enable etc.

The addresses used at time of writing are as follows:

X.1.4 = 1. I/O - 0317.03

X.4.0 = 2. I/O - 0317.03

X = KE address = 4.0.0

4 1/0 0318

The I/O is used to control the magnetic tape cassette.

4.1 I/O Assignment

Bit 12	EG 0.0	EG Y.1 code error	EG Y.2		EG Y.3		EG Y.4	EG Y.5	AG 0.0	AG Y.1	AG Y.2		AG Y.3		AG Y.4	AG Y.5
=	* 168	read bit number error	ed	01		93	3878	do I		in i cter	he IX6	es do				
10	E 1988	read parity error				61	b di	ie do	best best	ionar igno:	0	HT dis				
6	-5 6 98000	RAL	Bit 9			8 8	ime nift	esd le s lion	t s to gree	si i s ii o bi	Bit 9	,				
80		buffer	Bit 8	2000 000	00 29	1	tim bift pera	ite ne s ce o	e s i be	ai i	Bit 8					
7		CRC	Bit 7		п		0 86			etio Sita	Bit 7					7.00
9		time	· Bit 6	input data		3.8	1990	318		nq i	Bit 6				3	200
5		write parity error	Bit 5	rta			deck	ed) tion		control code of deck	Bit 5	output data			. Open	ntrol code ch
4	5 DB	end of operation	Bit 4		Bit 8		dni	esin	- I/O card address	of deck —	Bit 4	8	Bit 8		542	control code change mechanism
3	ni h	write inhibit	Bit 3	63	Bit 7	ndui	aad	eject container full	d address –	d in Bas Bas	Bit 3		Bit 7	 output data 		a msir
2		end of tape	Bit 2		Bit 6	input data —	5eat	change process is running	edre	13.33 STC	Bit 2		Bit 6	ata		41
-		ready	Bit 1		Bit 5		d eu	hopper empty	0=cassette 0 1=cassette 1	0013	Bit 1		Bit 5			ž ā

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4.1.1 Description of I/O Assignment

 $\boldsymbol{3}$ input and $\boldsymbol{4}$ output instructions are required to control the cassette.

4.1.1.1 Input Instructions

EG X.Y.1	Interrogate status bits
Bit 1	Ready
	The cassette is ready to operate.
Bit 2	End of tape
	The end of tape has been detected in the cassette.
Bit 3	Write inhibit
	There is a write inhibit for the actual cassette in the deck.
Bit 4	End of operation
	A write or read operation has been completed.
Bit 5	Write parity error
	A parity error has been detected during a write operation.
Bit 6	Time error
	There is a write time error if the 4-character buffer and the shift register become empty during a write operation.
	There is a read time error if the 4-character buffer and the shift register become full during a read operation.
Bit 7	CRC error
	The computed check character differs from the read in check character (check character = CRC character).

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MPUTER undendienst		8870/2/4/6
Bit 8	Buffer status	
	This bit provides information cond status of the 4-character buffer.	cerning the
	"Read" operation: The bit is set first character mitted to the buffer. If remaining as the burcharacters.	r is trans- 4-character ains set as
	"Write" operation: The bit is set are 4 character 4-character but full).	s in the
Bit 9	RAL reader	
	connected.	ader is
Bit 10	Parity error	
	A parity error has occurred during operation.	g a read
Bit 11	Bit number error during read	
	During the read operation a data other than the 9-bit character hadetected.	character s been
Bit 12	Code error torrago ragino	YXX DX · ·
	The outputted control code is not the cassette transport.	valid for
• EG X.Y.2	Interrogate input data for 8-bit processing.	character
	These bits contain the code of th character.	e input
Bit 10	Not applicable	
Bit 11	Track location	
	This bit denotes whether the A or the cassette is being used. Not u 900 Ml and the 8870.	B side of sed for the
Bit 12	Bit 12 denotes whether an operati completed without any fault.	on was
	Bit 12 = "1" = Operation sati Bit 12 = "0" = Operation unsa	

8870.

This bit is not used for the 900 Ml and the



object style of the style of th

EG X.Y.3 Interrogate input for 4-bit charcter processing (system 820 only).
 This input instruction is not used for the 8870 (8-bit processing only).

• EG X.Y.5 Status bits for cassette RAL reader.

Bit 1 Hopper empty

Bit 2 Change process is running

Bit 3 Eject container full

4.1.1.2 Output Instructions

• AG X.Y.O Preselection of I/O 0318 and connected cassette.

Bit 1 Bit 1 selects one of the two cassettes connected to the I/O for the next I/O operation.

Bit 1 = "0" = the first cassette of the I/O
 is selected.

Bits 2 - 4 These bits contain the preselection address for the I/O 0318 to be addressed.

• AG X.Y.1 Output control code for cassette drive.

Table of control codes

Control	Instruction
0.0	Stop operation
0.3	Write check character
0.5	4-bit data format changeover
0.6	8-bit data format changeover
0.9	Clear status detector
3.0	Open cover
3.3	Reset one block without erase
3.5	Run forward to BOT without erase
3.6	Rewind to leader tape
3.8	Pay off
3.9	Read block
6.3	Reset one block with erase
6.5	Run forward to BOT with erase
6.8	Write block with long block gap
6.9	Write block with normal block gap

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•	AG X.Y.2	Output data characters for write operation.
		This instruction loads the output character into the 4-character buffer of the I/O.
•	AG X.Y.3	This instruction is used only for 4-bit character processing (820 system).
•	AG X.Y.5	Control code for change mechanism.
		Output control code for change mechanism of cassette RAL reader.
		Control code Instruction 3.0 Retract head, cover open

4.2 Interrupt Release

The I/O 0318 cannot be interrupted and is controlled by the clock interrupt.

Unlock and rewind

4.3 Addressing

The preselection address and the I/O address are used. The instruction AG X.Y.O is used for the preselection address, the selection address being in bits 1 to 4.

The I/O address used at the time of writing is X.C.0. X = KE 2802 address (= 4.0.0)

I/O	Address	Pre-Selection
1. I/O	12.12.0	0.0 or 0.1
2. I/O	12.12.0	0.2 or 0.3

3.3



200-20-70-70-70-

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5 1/0 0325

5.1 I/O Assignment for Printer 4550.03 with Genuine DP Electronics and 0817.01

	*	, 83	, a	× 11 1	ant Å	i ugs
-	end of paper	0	end of paper	0	Data 1	Data 1
2	8823	84 ER	10.8	(A %	Data 2	Data 2
es.	Select	0	Select	0	Data 3	Data 3
4	Busy	Data	Busy	Data	Data 4	Data 4
5	feed	-	Vorschub	-	Data 5	Data 5
9	1G 3	50 0	ed n	0131	Data 6	Data 6
Z 7	Light	ts 1	Light	- 80 a	Data 7	Data 7
80	Safety switch	-	Safety switch	-	Data 8	Data 8
6	rano	10	ioti	wa ,	Strobe	Strobe
10		0J 8) X		bur na A	1023	6.1
LAG	0	- 9779	o pal	nol:	Paper Instr.	Paper Frstr.
12	Fault	0	Fault	0		
Bit	EG X.Y.1	EG X.Y:1	EG X.Y.2	EG X.Y.2	AG X.Y.1	AG X.Y.2

1 1, printer #2 2, printer #3 1, printer 0817.01 0817.01 0817.01 0817.01 0817.01 0817.01 0817.01 0817.01

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5.1.1 Description of I/O Assignment

(When cable 7032.03 is used for connection of printer 4550.03 and 0817.01).

There are 2 input and 2 output instructions.

5.1.1.1 Input Instructions

EG X.Y.1 Interrogate printer 455.03 status bits.

Bits 1 - 3 Not used

Bit 4 Data demand, equivalent to "request" signal.

Bit 5 Always "1"

Bit 6 Not used

Bits 7 and 8 Always "1"

Bits
9 and 10 Not used

Bit 11 Always "1" (Recognition bit for printer 0817.01)

Bit 12 Not used

• EG X.Y.2 Interrogate printer 0817.01 status bits

Bit 1 End of paper

Bit 2 Not used

Bit 3 Printer select bit, switch printer to on-line

Bit 4 Busy, printer ready to operate

Bit 5 Paper feed is running

Bit 6 Not used

Bit 7 Light defect (positioning error), only when the positioning lamp is defective.

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8870/2/4/6

Safety switch indicator on right hand side of Bit 8 carrier (no longer fitted for some time, therefore always "1"). ling feed for

Bits 9 and 10

Not used

Bit 11

Distinction bit for printer 0817.01 (Bit 11 = "0") and printer 4550.03 (Bit 11 = "1")

Fault Bit 12

Printer hardware fault

5.1.1.2 **Output Instructions**

- Output printer characters, control characters AG X.Y.1 and feed information for printer 4550.03.
 - Output information bits Bit 1 - 8

A data character or a control character may be outputted.

Control character

Symbol	Code	Meaning
CR		Print release
LF	0.10	Line switch
FF	0.12	Line switch by channel feed

Strobe bit Bit 9

> Each information item in bits 1 to 8 is outputted once with the strobe bit and once without the strobe bit.

Strobe = Information transfer signal.

Bit 10 Not used

Bit 11 Paper instruction bit

> If bit 11 is set there is line feed information in bits 1 to 8. Bit 5 is used to differentiate between line feed and channel feed. Line feed information in bits 1 to 4 and in bits 6 and 7.

Bit 5 = "0": Implement line feed (63 lines max.)

Bit 5 = "1": Implement channel feed (channel number in bits 1 to 4)

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Bit 12 Not used

• AG X.Y.2 Output print character, control character and line feed for printer 0817.01.

See AG X.Y.1 for bit assignment.

5.2 Interrupt Release 50.0000 assisting to the Contract of the

The I/O 0325 cannot be interrupted and printer control is via the clock interrupt.

5.3 Addressing

Bits 5 to 8 of the address to be outputted are used. At the time of writing address X.D.1 is used. X = KE 2802 address

Famer instruction bit

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I/O Assignment for Data Product Printer 4552 with Nixdorf Electronic Equipment

READY L DANFN щ PAEN ш 4 a dalling en H DAME = "8" while the pri 9 4 Z 00 ш DASTRN 6 and deliaming in an acade cheracter and instruction 0 Instruction scharacter codes Seed only 5003 11 beet enid 12 Bit

AG X.Y.1 EG X.Y.1 Row

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5.4.1 Description of I/O Assignment using Connection Cable 7032.02

There is one input and one output instruction.

5.4.1.1 Input Instructions

- EG X.Y.1 Interrogate printer status bits.
 - Bit 1 READY

The printer is ready to operate.

Bit 2 DANFN (Data request)

Data request is the acknowledge signal for the transfer of characters and instructions to the printer. It is "l" (DANFN = 0V) if the printer is waiting for data. After each transfer of a character (DASTR) DANF becomes "0" for at least 250 ns.

DANF = "0" while the printer is printing.

DANF = "1" when the printer paper feed is operating and data can be transferred

In principle data can only be transferred to the printer if DANF has previously been interrogated as "1".

Bit 3 PAEN

End of paper (lower switch).

5.4.1.2 Output Instructions

- AG X.Y.l Output information
 - Bits 1 7 These are information bits and contain the character and instruction codes for the printer.

Instruction character codes

Symbol	Code	Meaning
CR	0.13	Print release
LF	0.10	Line feed
FF	0.12	Line feed by channel feed

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Bit 8

If bit 8 is set then there is line feed information in bits 1 to 7. The content of bit 5 determines whether line or channel feed is carried out.

Bit 5 = "1": Line switch (63 max).

Bit 5 = "0": Channel feed (channel number in bits 1 to 4)

Bit 9

Strobe bit, information transfer bit.

Each information item is outputted once with the strobe bit and once without the strobe bit.

5.5 Interrupt Release

10 to 12 Not used

The I/O 0325 cannot be interrupted. Printer control is via the clock interrupt.

5.6 Addressing

Bits 5 to 8 of the outputted address are used. At the time of writing the address X.D.1 is used (X = KE 2802 address).



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For notes I all a set then there is line I and in the set of bid in information in bits I to 7. The content of bid is a determined whether line of channel feed is carried out.

Bit 5 = "I": Line switch (61 max)

Rit 5 = "0": Charmel feed (channel number in bits 1 to 4)

Strone bit, information transfer bit

Each information item is outputted once with the atrope bit and once without the stroke bit

Bits or or a

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The I/O 0325 cannot be interrupted. Frinter control is via the class interrupt.

5.6 Addressing

hits 5 to 8 of the outputted address are used. At the time of writing the address X.D.1 is used (X = KE 2002 address);

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6 1/0 0327

The I/O 0327 is used to control the daisy-chain line.

6.1 I/O Assignment

a 1	e 1 data bit	ai i	3.5.4	1 = comm. 0 = Term.	31138	terrogate st ceived chara		
a 2	e 2	M2 parity error	j be	Reset M 2	1,5	e parity bit		
в С	ه د	M3 transfer taking place	E.A	8 0	g 61	atus bits S itus bits		
a 4	4 4	M4 ANB≙ rdy. call	ı,	atio UST)	- IDN	In the coss control uni		
a 57	و ت	eran ALLE Voas	data bit	2008		100 100 POLICE PORT PORT PORT PORT PORT PORT PORT PORT		
а 6	9 9	eady eady		\$0 ₁ 1_	lani	Selected.		
a 7	e 7	193 1116 1011			0 = Select 1 = Poll			
8 8	e 8 data bit	08.2 m		508 5010	for OP code 0 = Select with local 1 = Poll	MINT BOILDS		
9 9	e 9 parity bit	en i i i	eg b	eni e	183	Selected Data charac		
a 10	e 10 status bit S 10	Ton		laci	eno São	Acknowledge		
a 11	e 11 status bit S 11	300		8	lavi.	(NUSS) cece Character		
a 12	e 12 status bit S 12	M12="1" send buffer busy		133	110	misses eff		
Bow	1.7	EG Y.2 s	AG Y.1	AG Y.2	AG Y.4			



6.1.1 Description of I/O Assignment

There are two input and three output instructions.

6.1.1.1 Input Instructions

• EG X.Y.l Interrogate status bits and input data.

Bits 1 to 8 Received character

Bit 9 The parity bit allocated to the received character.

Bits
10 to 12 Status bits S 10 to S 12
Meaning of status bits

In the communications In terminal control unit (DUST) S 12 S 11 S 10 or garbled POLLcharacter procedure character 0 0 SELECTreceived on line Does not ready to Polled transmit happen Terminal not 1 0 0 Selected ready to receive or a terminal parity error is detected Polled-Does not Terminal not ready to happen 0 1 1 operate Selected Data character A character with contained parity 0 1 1 incorrect error parity was Acknowledge character received The communications control unit A correct character (DUST) received a correct character was received 0 The terminal received a character correctly

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• EG X.Y.2 Interrogate flag bits 100100 A.Y.X DA

Bit 2 Flag bit 2 Telegraph Seemble 8 of 1 alls

A parity error has ocurred during data transfer.

Bit 3 Flag bit 3

A data transfer process is taking place.

Bit 4 Flag bit 4

the I/O is ready for receiving. Applies in the "DUST" and "Terminal" operating modes.

Bit 4 is reset when an address character is detected on the line (no longer ready for receiving).

Bit 12 Flag bit 12

The send buffer is busy.

6.1.1.2 Output Instructions

- AG X.Y.1 Load data characters into send buffer.

 Bits 1 to 8 Data characters to be outputted.
- AG X.Y.2 Output operating mode

Bit 1 = "0": The I/O is switched to the "Terminal" operating mode, i.e. is passive.

Bit 1 = "1": The I/O is switched to the "DUST" operating mode, i.e. is active.

Bit 2 Reset M2

The "parity error" flag is reset.

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• AG X.Y.4 Output address character

Bits 1 to 6 Address character to be outputted.

Bit 7 This bit determines whether a data character is to be transmitted or a data character is to be received after the address which has been transmitted.

Bit 7 = "0": A data character is received after the address character has been transmitted (select).

Bit 7 = "l": A data character is transmitted after the address character has been transmitted (poll).

Bit 8 This bit determines whether characters are transmitted singly or in sets.

Bit 8 = "0": Transmission of single characters Bit 8 = "1": Transmission of character sets Only possible with local data transmission.

6.2 Interrupt Release

The I/O 0327 cannot be interrupted and is controlled by the clock interrupt or by an external I/O interrupt, e.g. I/O - 1806 interrupt.

6.3 Addressing Time at Olited 180 # 1 118 1 118

Bits 5 to 9 of the address to be outputted are used to address the I/O. At the time of writing the address 1.9.0 is used for the first I/O and the address 1.A.0 is used for the second I/O. (Remember the KE 2802 address).

The "barity error" riad is remet.

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The I/O 1801 is used to control low-speed peripheral devices such as the card reader, the card punch, the tape reader and the tape punch. The assignment of the I/O therefore depends on the connecting cable used (see various connecting cable types).

7.1 I/O 1801 Addressing

The I/O 1801 is addressed by means of preselection and the board address.

Preselection is via the instruction AG 0 with bit 11 set and the board number in bits 1 to 4.

• Board preselection a space pathog

								_	-	_	-		Contract of the contract of th	
AG 0	12	11	10	9	8	7	6	5	4	3	2	1	Bit	
	0	1	0	0	0	0	0	0	X	X	X	X		
							196 197 3						_I/O	board

The I/O address used at the time of writing is 4.A.X.

4.0.0 = KE address

0.A.0 = I/O 1801 address

X = Line address

7.2 Interrupt Release

The I/O 1801 does not generate any internal interrupt and can only evaluate interrupts from peripheral equipment (set internal interrupt flags) and inform the central processing unit (interrupt channel). A total of 4 interrupts can be stored.

Interrupt flags (interrupt channels) can be disabled or enabled by means of instruction AG 0 with bit 12 set.

12	11	10	9	8	7	6	5	4	3	2	1	Bit
1	0	0	0	0	0	0	0	X	X	X	X	
									-	<u></u>		Interrupt
												disable bits

Interrupt disable bit = "1": Implement interrupt disable.
Interrupt disable bit = "0": Cancel interrupt disable.



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Interrupt assignment for the 120-pin Ericsson connector of the I/O 1801.

Signal path	A99	A94	A89	A84	A79	A74	A69	A64
Interrupts	4B	4A	3B	3A	2B	2A	1B	1A
	4. Int	errupt —	3. In	terrupt —	2.10	terrupt —	1.Int	errupt

The letters A and B indicate whether the interrupt request from the peripheral egipment is triggered by the negativegoing or the positive-going edge of the pulse.

- A = Request triggered by the negativegoing edge of the pulse.
- B

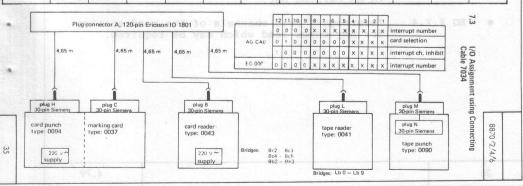
- Request triggered by the positivegoing edge of the pulse.
- A and B together
- Request triggered by both the positive-going and negative-going edges of the pulse.

The request for the interrupt bit is a result of the input instruction EG 0.

enabled by means of instruction AG C with bit 12 cor.

reserve all rig its contents (c n act, literary p stration of desi uction without

	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
EG 4.A.1	tape reader no inter,	tape reader tape change	tape reader framing pulse 2	tape reader framing pulse 1	tape reader channel 8	tape reader channel 7	tape reader channel 6	tape reader channel 5	tape reader channel 4	tape reader	tape reader	tape reader
Signal path	A 56 Lb 1	A 51 Lc 0	A 46 LA 0	A 41 La 9	A 36 La 8	A 31 La 7	A 26 La 6	A 21 La 5	A 16 La 4	A 11 La 3	A 6 La 2	A 1 La 1
EG 4.A.2	card reader no inter.	card reader multi-punch ing ch.11-7	card reader reaming pulse 2	card reader framing pulse 1	card reader	card reader	card reader	card reader	card reader	card reader	card reader	card reader
Signal path	A 57 Ba 0	A 52 Bb 2	A 47 Ba 2	A 42 Ba 1	A 37 Bb 1	A 32 Ba 6	A 27 Ba 9	A 22 Ba 8	A 17 Ba 7	A 12 Ba 5	A 7 Ba 4	A 2 Ba 3
EG 4.A.3	tape punch end of paper punch error	TZL Ready	tape punch pilot hole	tape punch timing	136112	10400	card punch change punch magnet	card punch card in read station	card punch card in punch station	card punch submit inhibit	card punch switch off card feed	card punch punch inhibit
Signal path	A 58 Mc 3, Nc 3	A 53 Bb 8	A 48 Ma 0	A 43 Ma 1	A 38	A 33	A 28 Hc 4	A 23 Cb 3	A 18 Hc 7	A 13 Hc 6	A 8 Hc 5	A 3 Hc 1,Hc 8, 9
EG 4.A.4	card punch channel 12	card punch channel 11	card punch channel 0	card punch	card punch	card punch channel 3	card punch channel 4	card punch channel 5	card punch channel 6	card punch channel 7	card punch channel 8	card punch channel 9
Signal path	A 59 Cb 2	A 54 Cb 1	A 49 Ca 0	A 44 Ca 1	A 39 Ca 2	A 34 Ca 3	A 29 Ca 4	A 24 Ca 5	A 19 Ca 6	A 14 Ca 7	A 9 Ca 8	A 4 Ca 9
EG 4.A.5	03.63	aggod s av	ana n	edw 6	npakta	i a.	sotios when	scani Voca	ainT e ai			
Signal path	A 60	A 55	A 50	A 45	A 40	A 35	A 30	A 25	A 20	A 15	A 10	A 5
AG C.A.1				tape punch release	tape punch punch magnet 8	tape punch punch magnet 7	tape punch punch magnet 6	tape punch punch magnet 5	tape punch punch magnet 4	tape punch punch magnet 3	tape punch punch magnet 2	tape punch punch magnet 1
Signal path	A 116	A 111	A 106	A 101 Mb 9	A 96 Mb 8	A 91 Mb 7	A 86 Mb 6	A 81 Mb 5	A 76 Mb 4	A 71 Mb3	A 66 Mb 2	A 61 Mb1
AG C.A.2	LSL Start	LSL Stop		card reader feed magnets	101 90	D F-SW		. (3)	card punch step off	card punch step on	card punch card feed	card punch motor
Signal path	A 117 Lc 1	A 112 Lc2	A 107	A 102 Bc 6	A 97	A 92	A 87	A 82	A 77 Hb 7	A 72 Hb 8	A 67 Hb 4	A 62 Hb 3
AG C.A.3	card punch punch magnet 12	card punch punch magnet 11	card punch punch magnet 10	card punch punch magnet 9	card punch punch magnet 8	card punch punch magnet 7	card punch punch magnet 6	card punch punch magnet 5	card punch punch magnet 4	card punch punch magnet 3	card punch punch magnet 2	card punch punch magnet 1
Signal path	A 118 Hb 2	A 113 Hb 1	A 108 Ha 0	A 103 Ha 1	A 98 Ha 2	A 93 Ha 3	A 88 Ha 4	A 83 Ha 5	A 78 Ha 6	A 73 Ha 7	A 68 Ha 8	A 63 Ha 9
Interrupt		edi n	Arec	a si	4 B	4 A	3 B	3 A	2 B	2 A	1 B	1 A
Signal path	A 119	A 114	A 109	A 104	A 99	A 94	A 89 Ma 1	A 84 Ma 1	A 79	A 74 Lc 4	A 68	A 64 Bb 5
Power supply	0 V	0 V	0 V	0 V	+ 36 V	+ 36 V	+ 24 V	+ 6 V	Mess	30 V		
7	A 120	A 115	A 110	A 105	A 100	A 95	A 90	A 85	A 80	A 75	A 70	A 65
	Hb 0 3x Cb 0 3x Bb 0 2x Bb 4 2x	bauq i	imul do	jxan	Hb 5 2x Bc 4 2x Bc 5 2x	befor	Hb 9 2x Bb 9 2x	Cb 6 2x	RidT			



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7.3.1 Description of I/O Assignment for Card Punch 0095.00 or 0095.01

The punch is connected to the I/O 1801 via cable 7034. Two input instructions and two output instructions are required to operate the punch.

7.3.1.1 Input Instructions

•	EG	X.Y.3	Interrogate	punch	status	bits
---	----	-------	-------------	-------	--------	------

Bit 1 Punch inhibit

This instruction is inputted when the hopper is empty, when the stacker is full, when a card is being fed and when the manual card release control is actuated and the motor is running up (after switching on).

Bit 2 Switch off card feed

Cancel card feed magnet (switch off coupling magnet).

Bit 3 Submit inhibit

This bit is set up to the end of the card feed operation.

Bit 4 Card in punch station

This bit is set when there is a card in the punch station.

Bit 5 Card in read station

Message from read channel 13 (card in read station).

Bit 6 Change punch magnet

This bit is set before the next column punch to be carried out.

• EG X.Y.4 Interrogate read channels of the read station for any check read which may be required.

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7.3.1.2 Output Instructions E0.6300 tehes 8 the 3 tot manuspace OV AT

AG X.Y.2 Output operating mode bits to make the same to the s

Bit 1 Motor on Walled Delpedon al rebest suff

This bit is outputted to start the card punch motor. (There is a delay whilst the motor runs up and punch inhibit is implemented during this period).

Bit 2 Card feed

This bit addresses the coupling magnet and releases a card feed.

Bit 3 Step on Albanda ashbas bran

This bit switches on the step-by-step transport of a card through the punch station.

Bit 4 Step off

This bit switches off the step-by-step transport of a card through the punch station (after the last column has been punched).

AG X.Y.3 Output punch information

7.3.2 Interrupt Release and bases out not not not not the Control of Sans Re

The punch does not release any interrupts and is controlled by the clock interrupt.

7.3.3 Addressing and the Honor of the Lord and and and

See Section 7.1.

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7.4 I/O Assignment for Card Reader 0043.03

7.4.1 Description of I/O Assignment

The reader is connected to the $\rm I/O$ 1801 via cable 7034. One input instruction and one output instruction are required to operate the reader.

7.4.1.1 Input Instructions

- EG X.Y.2 Interrogation instruction for acceptance of information and status bits.
 - Bits 1 to 3 These bits show the coded information from card reader channels 1 to 7.
 - Bit 4 Information from card reader channel 0.
 - Bit 5 Information from card reader channel 11.
 - Bit 6 Information from card reader channel 12.
 - Bit 7 Information from card reader channel 9.
 - Bit 8 Information from card reader channel 8.
 - Bits
 - 9 and 10 Indicator for the card reader framing bits.

Sequence of framing bits: 0, 1, 2, 3, 0, 1, 2, 3 etc.

- Bit 11 Multi-punch in channels 1 to 7, i.e. more than one hole is punched in columns 1 to 7.
- When this message is present the interrogation of read channels is not permitted.

7.4.1.2 Output Instructions

- AG X.Y.2 Output "start reader"
 - Bit 9 Bit 9 is used to "start" or "stop" the reader.

Bit 9 = "1": start reader Bit 9 = "0": stop reader

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7.4.2 Interrupt Release

An interrupt is released to inform the system each time a card column is read.

7.4.3 Addressing

See Section 7.1.

7.5 I/O Assignment for Card Reader 0041.01

7.5.1 Description of I/O Assignment

The reader is connected to the I/O 1801 via cable 7034.

One input instruction and one output instruction are required to operate the reader.

7.5.1.1 Input Instructions

- EG X.Y.1 Interrogate character information and status bits.
 - Bit 1 to 8 Read channel information from channels 1 to 8.

Bits

9 and 10 Framing pulses 1 and 2

Control signals for the recognition of individual rows of the punched tape. The status of these signals changes from row to row in the following sequence: 2, 0, 1, 3.

Bit 11 Tape change

This bit is set when a tape is in the read station.

Bit 12 No interrogation

When "no interrogation" is set the information contained in bits 1 to 8 must not be evaluated since new information is actually being loaded into the buffer.



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7.5.1.2 Output Instructions

AG X.Y.2 Output operating mode bits

Bit 1 Stop

Switch off motor and switch on reader coupling

(the read process stops).

Bit 12 Start

Output motor and reader coupling (reader

starts).

752 Interrupt Release

An interrupt is released when the buffer contains new data which can be transmitted to the system.

7.5.3 Addressing

The I/O 1801 is used for addressing purposes (see Section 7.1).

I/O Assignment for Tape Punch 0090.00 7.6

7.6.1 Description of I/O Assignment

The tape punch is connected to the I/O 1801 via cable 7034. One input instruction and one output instruction are required to operate the tape punch.

7.6.1.1 Input Instructions

EG X.Y.3 Interrogate tape punch status bits.

Tape punch timing Bit 9

This bit is set when a punch process is taking place. When it is not set the next item of punch information can be outputted.



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Bit 10 Pilot hole

This bit is required when processing edge punched cards. It signals the end or beginning of an edge punched card.

Bit 11 Not used

End of paper, punch fault
This bit is set when the feed spool is empty
or when the take-up spool is full.

7.6.1.2 Output Instructions

Bit 12

AG X.Y.1 Output punch information
 Bits 1 to 8 Output punch information

1 to 8.

Bit 9 Release

The coupling magnet is addressed, bit 9 must always be outputted in conjunction with bits

7.6.2 Interrupt Release

The tape punch is interrupt-controlled. Interrupt release is via the "tape punch timing" signal (bit 9 of EG X.Y.3).

7.6.3 Addressing

See Section 7.1.

7.7 I/O Assignment of the 1801 when used to Control Mark Reader, Connected via Cable 7031

Row Bit 12 11 10	E6 Y.1	Signal path	EG Y.2	Signal path	EG Y.3	Signal path	EG Y.4	Signal path	AG Y.1	Signal path	AG Y.2	Signal path	AG Y.3	Signal path	Interrupt	
6												L	S a	9.Î.	roe B	The second secon
80	Doc. Reject	A36, La7	Line Reject	A.37, La6	K16	A38, La6	80 ¥	A39. Lc8						20	4 8	
7	Doc. Present	A31, La3	Doc. Vor.	A32, Lc11	K15	A33, Lb5	K 7	A34, Lc7		83			ions ions		4 A	THE PROPERTY OF THE PARTY OF TH
9	no inter- rogation	A26, La5	ML fault	A32, Lc11 A27, La12	X 41	A28, Lb4	У 9	A29, Lc6							8	Contract of the contract of th
5	Read Window	A21, La4	3 56	15	K13.	A23, Lb3	2 2 2	A24, Lc5	e LEqu	1.6 9.5 9.5					e A	
4	stacker	A16, La9	K20	A17, Lb10	K12	A18, Lb2	X 4	A19,Lc4	Select 2	A75		00	f,		28	Contract Compactures
3	Doc. Ready	A11, La8	K19	A17, Lb10 A12, Lb9	K11	A13, Lb1	ε ×	A14, Lc3	Select 1	A71,Lb11			inil To	00	2 A	
2	WT 2	A6, La2	K18	A7, Lb8	K10	A8, Lc10	K2	A9, Lc2,	Read	A71,Lb11 A66, La10 A62, La11					4 8	
-	WT1	A1, La1	K17	A2, Lb7	8 8	A3, Lc9	K1	A4. Lc1	Feed	A62, La11				EE	4	

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7.7.1 Description of I/O Assignment PRASSEL NOV DOC 118

Four input instructions and one output instruction are required to operate the mark reader.

7.7.1.1 Input Instructions

FC	X.Y.1	Interrogate	status	bits
LiG	VoToT	Tilleriogue	Deacas	200

B	its					
1	and	2	WT 1/WT	2		
			Signals	for	line	change

Bit 3	DOC READY
	This signal denotes that a document is present

Bit 4	STACKER
	This signal is transmitted when the stacker
	is full or the hopper is empty.

Bit 5	READ WIND	OW	
	Duration	of data	transmission.

Bit 6	No interrogation
	The information in channels 1 to 20 is not
	· binding.

Bit 7	DOC. PRESENT
	The document in question remains at the read station for the duration of this signal
	(length of document).

Bit 8	DOC. REJECT
	This signal is transmitted when there is a
	timing track defect or when a document
	being read is not straight.

	EC	v v 2	Interrogate	information	and	status	bits.
•	EG	X.Y.2	Interrogate	Intormation	anu	Status	DICD.

Bits	1	to	4	Channels	17	to	20
				Informat	ion	lin	nes

Bit 6 Er	ror	lamp
----------	-----	------

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DOC VOR (START 1) TO THE RESERVE OF Bit 7

Feed document as far as rocker 1. LINE REJECT

Bit 8

This indication is given for each line if marks are too faint. are too faint.

Interrogate information bits EG X.Y.3

Bits 1 to 8 Channels 9 to 16 Information lines

Interrogate information bits EG X.Y.4

Bits 1 to 8 Channels 1 to 8 Information lines

7.7.1.2 Output Instructions

AG X.Y.1 Output operating mode bits

Bit 1 FEED

Feed document from separator, document remains at CPS. moldepoined of

Bit 2 READ SET OF HOLLESTON SET

Read document in marker reader.

7.7.2 Interrupt Release

The mark reader is interrupt-controlled and and interrupt is released each time an information item is read. In addition the signal DOC. REJECT releases an interrupt. Tols signal is Wanshitted when there is a

Addressing and a state of the same and addressing

See Section 7.1.048 soldsmyothi adapottstal 3.7.8 as



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to	I/O is control	used the	2 1		COMP check characte error	seek end of error pos.	Till sidence di			310(3	
				-			nter —				
8.1		Assignment	m		sync	error	sector counter				
•	Input	assignment	4	888	E B	ready	Sec —				
			5	IR number	NAP1	air pressure present					
			9		LODA	First Seek	2200 bpi	Total 73		Ŧ	
			7		FSNR	split	Strobe		- 100 - 100		
			œ	100	FBNR	400 SP					
			6	30 34 22 24 25 25	KSTP				80		
			10		output	and the			63		
		E STATE OF THE STA	11	25 25 47	parity				1.8		
			12								
			13								
			14						1 2		
			15						1 2		
			16								
			Bit			drive no. 0	drive no. 0	drive no. 1	drive no. 2	drive no. 3	 ۲.
		36 36 36	Bi	EG 0.0.0.0.0	EG 0.0.X.0.1	EG 0.0.X.2.1	EG 0.0.X.2.2	EG 0.0.X.2.5 EG 0.0.X.2.6	EG 0.0.X.2.9 EG 0.0.X.2.10	EG 0.0.X.2.13 EG 0.0.X.2.14	EG 0.0.X.3.13

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Output assignment

0=enable 1=disable 0-delete 1-INT 0-DMA read here bit 5 is decimal and not hexadecimal 00-Arite 2 LMVG 3 head address track difference (n's complement) SZR 18 Bit 4 IR limit number interrupt number 2,5 MHz LO Restore Z 9 wind for-ward withcurrent reduct-ion FAR17 1 FAR18 forward FAGOS (n's complement -1) 00 FAR19 FAGOD 6 FAR 1 ... FAR 16 FKPOS FAR20 10 FLZ -12 0 -limit number 13 * œ 14 15 drive no. 0 f .on evinb T ,on evinb Bit AG 0.0.X.3.14 AG 0.0.X.3.15 AG 0.0.X.2.5 AG 0.0.X.2.6 AG 0.0.X.0.0 AG 0.0.X.0.0 AG 0.0.X.3.13 AG 0.0.X.0.2 AG 0.0.X.2.0 AG 0.0.X.0.3 AG 0.0.X.2.7 AG 0.0.0.0.0 AG 0.0.X.0.1 AG 0.0.X.2.1 AG 0.0.X.2.2 AG 0.0.X.2.3 Row,

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8.1.1 Description of I/O Assignment

There are 4 input and 9 output instructions for the I/O 1802.

8.1.1.1 Input Instructions

- EG 0.0.0 Interrogate interrupt number
- EG X.0.1 Interrogate status bits
 - Bit 1 CC comparison (CC comp.)

Bit l is set if the check character formed during a read operation differs from the check character read out from the track by the preceding read operation.

Bit 2 Read and compare error (LVG)

Bit 2 is set if the data read from a disk differs from the previously entered data during operation in the "read and compare" mode.

Bit 3 Synchronizing character not detected (SYN error).

Bit 3 is set if the synchronizing bit was not detected during a "read" operation with a specified time \triangle t after the reception of the required sector pulse (enable write permit).

 Δ t for 1.25 and 2.5 MHz operation = 200 us. The read operation is truncated and the I/O 1802 is cleared when a SYN error occurs.

Bit 4 Busy flip-flop

"Busy flip-flop" is set by the output instruction start (AG X.Y.3*) and can be restored by the following conditions:

a) When data traffic is completed normally (stop).

With the following causes of faults:
 Incorrect sector number
 Incorrect block number
 LOST DATA
 SYN error
 No stop
 Peripheral device power failure

b) When a positioning error is detected

* X = 1802 board address, Y = station address (2 for station 0)

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Bit 5

Power failure in peripheral device (NAP 1)

Bit 5 is transmitted if there is a power failure in a peripheral device. (Power failure in one of the connected magnetic disk stations.)

Bit 6

LOST DATA (LODA)

Bit 6 is set if an old I/O cycle runs when an I/O backplane request is made, i.e. when the cycle-stealing mode malfunctions. When this happens data exchange is terminated by the clear board signal.

The error message RU is included in the error message LODA, i.e. LODA is also set if RU is still present at the backplane after a period of 20 us because of a cycle fault.

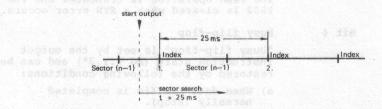
> The I/O 1802 is reset by LODA and the RU of the I/O 1802 is removed from the backplane.

Bit 7 Incorrect sector number (FSeNr)

Bit 7 is set if the desired sector is not detected within the period required to detect 2 index pulses (transfer of incorrect sector numbers).

Sector numbers are continuously transmitted from the addressed magnetic disk station (0564) to the sector counter register of the I/O 1802.

Worst case waiting time corresponds to the time taken for a disk to complete one rotation, i.e. 25 ms.



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Bit 8 Incorrect block number (FBINr)

Bit 8 is set if the I/O unit addresses a memory plug-in unit which is defective or is not present.

The criterion adopted is that within a specified waiting time (10 us approx.), which is greater than the access time of the memory, the memory start signal must be followed by a strobe reply signal. If this requirement is not fulfilled data exchange in the I/O unit is truncated by the board clear signal.

Bit 9 No stop noisosom ads dally golesiseno

Bit 9 is set if the index mark is overrun twice during the exchange of data. Such a fault originates in hardware and can occur if the stop signal, which should terminate normal exchange of data, is not generated or is ineffective. A magnetic disk which has already been started would not reply given such a hardware fault.

The I/O 1802 is also cleared in this case.

Bit 10 Output error (AG-error)

Bit 10 is set if an illegal output instruction (i.e. AG FAR, AG FLZ) is outputted on the I/O 1802 when the "busy flip-flop" /FB) bit is set.

All output instructions are illegal except the following:

The head address register (KAR) or the track difference counter (SPD) of a magnetic disk in which no exchange of data is taking place may be loaded. This enables other magnetic disk units to be positioned during the exchange of data (simultaneous mode).

If outputs are transmitted to the head address register or track difference counter of a magnetic disk unit in which exchange of data is taking place, these outputs will be identified as errors.

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The I/O 1802 reacts to illegal outputs as follows:

- a) The output instruction is received but is ineffective.
- b) Bit 10 is set. specified waiting time (10 us approx.), which

Bit 11 Parity error and setants at

Bit 11 identifies the reception of a byte from the backplane containing a parity error (this is only possible during "read and compare" or "write" in the 16-bit operating mode).

Conclusion With the exception of "busy flip-flop" (FB) all error indicators are set when the error in question occurs, and are reset when the next output instruction is outputted.

The errors LODA, FSeNr, SYN-fault, NAP 1 and no stop also immediately clear the I/O 1802 as well as the "busy flip-flop" signal. The I/O 1802 is also cleared when the NA signal is detected in the repeat mode.

- Interrogate status bits for magnetic disk EG X.2.1 station 0. MAN TOWN SUGGEO
- Bit 1 End of positioning

Bit 1 is set when a positioning operation has been completed.

Positioning fault paragrait Bit 2

Bit 2 is set if a positioning operation has not been completed within one second.

Bit 3 Error seld behavior the exchange oni tub

Bit 3 is set if any of the following errors are detected in the 0564.xx: Incorrect voltage, speed error, head selection error or an error during a write or read operation (see description of the 0564.xx). Bit 4 Ready

Bit 4

Bit 4 is set when the magnetic disk station is ready to operate.

Bit 5 Air pressure present

> Bit 5 is set when the magnetic disk station air pressure is present.



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Bit 6 3 10 First-seeks Juggue 1081 O'T 8.2.X DA 9

Bit 6 is set when a first-seek (first positioning after switching on) has been carried out.

Bit 6 is reset when the next restore instruction is outputted.

Bit 7 Split

Bit 7 is set when a split magnetic disk station is used.

Bit 8 400 SP

400 SP

Bit 8 is set when a 60 million byte magnetic disk station is used (60 million bytes = 400 cylinders).

8.1.1.2 Output Instructions

• AG X.0.0 Output interrupt number

Bit 12 = "0": The interrupt number to be outputted is in bits 1 to 8.

Bit 12 = "1": Bit 1 determines whether the I/O is disabled or enabled for interrupt operation.

Bit 1 = "1": Interrupt disable

Bit 1 = "0": Interrupt enable

• AG X.0.1 Load the field address register
Output address bits 1 to 16.

AG X.0.2 Load the field length counter

The field length is outputted as n = 1.

• AG X.0.3 Output sector number and address bits 17 to 20 for the field address register.

When sector number is outputted the sector being sought must be outputted as -1.

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AG X.2.0 I/O 1802 output instructions for test purposes

Bit 12 = "1"Bit 1 = "0"Bit 2 = "0" Clear instruction for the I/O 1802

Bit 12 = "1"]

Bit 1 = "1" Bit

Releases an interrupt in the

2 = "0" 1/0 1802

Bit 12 = "1"] Bit 1 = "0"

Releases the DMA cycle in the

Bit 2 = "1" I/O 1802

Output the track difference for magnetic disk AG X.2.1 station 0.

> The "track difference" is outputted as an inverted statement (complement).

- Output magnetic disk related data AG X.2.2
 - Bit 1 to 5 Head address

Bit 5 is decimal and not hexadecimal. Examole: Output head 14 = 1.4, Output head 10 = 1.0 etc.

Bit 6 Restore

> Current reduction Bit 7

> > From cylinder 128 with GA 1 and 3 and cylinder 256 with GA 0.

Positioning direction Bit 8

Bit 8 = "1": backwards

- Bit 8 = "0": forwards
- AG X.2.3 Output operating mode bits
 - Bit 1 Read
 - Write parable by all and roll 60
 - Bit 3 Read and compare
 - Bit 4 Changeover bit for 16-or 18-bit operation

Bit 4 = "0": 16-bit operation Bit 4 = "1": 18-bit operation

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Bit 5	Char	ige	109	er b	it fo	or write or	read	fre	equency	7
						frequency frequency				

Bit 6 Changeover bit for type of memory Bit 6 = "0": working memory (If bit 4 = "0" bit 6 is not evaluated i.e. a main memory is being addressed).

Bit 6 = "l": micromemory

Bit 7 Write leader tape without SYN-Byte The SYN Byte is replaced by a Null Byte. In conjunction with write (Bit 2) a whole track can be erased, i.e. entered as nulls.

Start FAGOS Bit 8 Data exchange without end of positioning interrogation and sector search.

Bit 9 FAGOD sector search without data exchange For test purposes only.

Bit 10 FKPOS Start of sector search without previous end of positioning interrogation.

Interrupt Release for Magnetic Disk Data Processing 8.2

The resetting of FB also serves as an interrupt release; this sets an interrupt message flip-flop. In addition each error bit which is set, except bit 11 (CC error) and bit 2 (LVG) releases an interrupt.

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8.3 Addressing

Address bit assignment

Bits y money to agyr and aid sevenpend?

1 and 2 I/O line number

Bits 3 to 5 Magnetic disk unit number (if bit 6 = "1")

Bit 6 If bit 6 = "0" all registers, which can be loaded or interrogated independently from the magnetic disk unit number, are addressed (i.e. only the register of the I/O 1802).

If bit 6 = "1" all registers, which can only be loaded or interrogated depending upon the magnetic disk unit number, are addressed.

(For exception see AG 0.0X.2.0)

oBits trace to hee ducativ epastaxs stad

1 to 11 I/O 1802 address

Bit 12 Bit 12 = "1" for all output instructions.

Bits

13 to 18 Contain "0" when the I/O is being addressed.

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9 DMA 1804

The DMA is used to control high-speed peripheral devices.

9.1 I/O Assignment

Bit	EG 0.0.0.0.0	EG X.0.2	EG X.0.3	EG X.0.4	EG X,0.8 – EG X,15.15	AG X.0.0	AG X.0.1	AG X.0.2	AG X.0.3	AG X.0.4	AG X.0.5	AG X.0.6	AG X.0.7	AG X.0.8 – AG X.15.15	000000
18	108	det	ej T	erro	omi	1 4	1 3	PR S	1 4	Fig					_
11							5-2 5391								
16							1.1 . 2 38 . A	90 S		iia sub sine					
15							one	E 30		MY					
14							tuo ,	r al ed.		inp soo					Jumos
13							. 1 68 9 n.a	er a		ela edd					to limit
12			300 1578	special chars.	3 81 81	disable enable	block &	prog valu on	503 5 0	liw ego		for code 0	delete special chars.		sodonia simil osolomoo
=			1	BLZO	lanoi	disable and enable INT no.	block address counter	8036	30	will.		for BLZ			
10			100	FVPD	1 8	oold sula	ounter	in enta	inea melij	sta			delete delete BLZO FVPD		
6	irgn Hevi	9591 9591	03.83 00.10 03.8	FZDP	lds lds	neja: Sija:	ies plbn p lo	re i ber	900 90 U	start of code table register			delete FZDP	ס	
∞			block		dynar		(0	E) 40	rflo	e table r		1	ZUP	dynamic output	
7	auj	ran)	block length counter	FVPD	dynamic input	inte	atus	group s address	block Ie	egister	group s table	SSP	delete	output	
9	nterrupt	original character register	ounter	FZDP DEA	a sh	interrupt number register	90.9	group selection block address	block length counter	8 0 8	group selection code table	count back- wards	98	8	=
5	number	Sharacte	16.13 31.63	BLEN	d a	mber re	M A	block	unter	D 6	code	data transp. despite PAINT			
4	interrupt number register	register .	isse tect	time error mem.	163	gister	io i chai	block	l 16 Sege		code	read mem. off			
3		1 4 2 3 4 A		VPC er error ar mem.	- A-	a for	ars. F	block address counter	ajai	per per	code table register	forr			
2	idmu ido	1.3	en sa	end of area not r.	30	0.0		counter	0118		ister	format change	28	- 80 - 60	
-				over- flow		dis,=1 en,=0						agu			188

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9.1.1 Description of I/O Assignment

DMA Input and Output instructions.

9.1.1.1 Input Instructions

- EG X.0.0 Interrogate the interrupt channel number.
- the original character register.

 the original code of a character is entered in the original character register if null (= special character) is detected when working with the DMA internal code transcription when
- EG X.0.3 Read out the content of the block length counter register.

a character code has been transcribed.

- EG X.0.4 Read the status of the markers (status details).
 - Bit 1 Overflow (BÜ)

 If bit 1 is set more characters were received than were indicated in the block length counter. The number of extra characters received is present in the block length counter as a complementary value.
 - Bit 2 End of area not reached (BU)

 If the program loads the block length counter

If the program loads the block length counter with a value bit 2 is set (start of DMA operation = independent data traffic).

Bit 2 is reset, i.e. cleared, if the value of the block length counter is null when an input or an output operation has been completed.

Bit 3 VPC error memory (parity error)

Bit 3 is set if a parity error is detected during a DMA memory cycle. The DMA operation which is running is truncated.

Bit 4 Time error memory

Bit 4 is set if a time error is detected during a DMA memory cycle. The DMA operation which is running is truncated.

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Bit 5 BLEN (negated block length end generator)

named Alica Bit 5 is set when the block length counter is loaded.

Bit 5 is deleted when a DMA input or output operation has been satisfactorily completed on the PSP end, i.e. for an input the block length end signal is detected on the PSP or, for an output, the block length counter is null.

Bit 11 = "1": BLZO block length counter equal to null.

Bit 6 FZDPDEA (error message for time error in DMA and peripheral device during data input or output).

Bit 6 is set if a time fault is detected in the PSP during DMA data transmission (input or output) between DMA and peripheral device. Time monitoring = 10 us.

Bit 7 FVPDDE (error message or VPC parity error in peripheral device and DMA during data input).

Bit 7 is set if a parity error is detected in the PSP during DMA data traffic (input) between peripheral device and DMA.

Bit 8 Not used

Bit 9 FZDPDY (error message for time error in DMA and peripheral device during a dynamic input or during interrupt interrogation of peripheral device).

(Dynamic input or output is equivalent to input or output controlled by the central processing unit).

Bit 9 is set if a time error is detected in the PSP during a dynamic input or output or during interrupt number interrogation of peripheral device (by means of the instruction EG 0).

Bit 10 FVPDDY (error message for VPC parity error in peripheral device and DMA during dynamic input or during interrupt interrogation of peripheral device).

Bit 10 is set if a parity error is detected in the PSP during dynamic input or during interrupt number interrogation of peripheral device.

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Bit 11 BLZO (interrupt flag for block length end).

Bit ll is set if the block length counter assumes the value null during DMA traffic (output). When bit ll is set this can release an interrupt if required, provided that bit 11 was previously outputted on AG 6.

Special character bit Bit 12

Bit 12 is set, during DMA traffic, the information null is detected after code transcription. The code of the original character is stored in the original character register.

When bit 12 is set this can release an interrupt if required, provided that bit 12 was previously outputted on AG 6.

Output Instructions and of a pairotinom smit 9.1.1.2

This instruction loads the interrupt register. AG X.0.0

Bit 12 and 11 = "0": The interrupt number is outputted in bits 1 to 8.

Bit 11 = "0":

Bit 12 = "1" and Bit 1 determines whether the interrupt is inhibited (Bit 1 = "1") or enabled (Bit 1 = "0")

- AG X.0.1 Load the block start address counter register.
- AG X.0.2 This determines with which type of memory (HA, Mi or AR) the DMA communicates:

Bit 5 = "1": Micromemory (Mi) Bit 6 = "1": Working memory (AR) Bit 7 = "1": Main memory (HA)

- AG X.0.3 Load the block length counter register. Meldon deal of lo This instruction simultaneously instructs the DMA to initiate automatic data transmission.
 - AG X.0.4 Load the start of code table register.

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 AG X.0.5 This instruction determines in which memory the code table is located.

Bit 5 = "1": Micromemory (Mi)
Bit 6 = "1": Working memory (AR)
Bit 7 = "1": Main memory (HA)

AG X.0.6 Set the operating mode flip-flops

Bit 1 = "1":

Bit 2 = "0":

Bit 3 = "0":

Bit 1 = "0":

Bit 2 = "0":

Bit 2 = "0":

Bit 3 = "0";

Bit 1 = "1";

Bit 2 = "1";

Bit 3 = "0";

2 x 8-bit data format with code transcription

Bit 4 = "0": Data transfer is from the peripheral device to the memory.

Bit 4 = "1": Data transfer is from the memory to the peripheral device.

Bit 5 = "1": Data transfer is not interrupted by any parity errors which may occur.

Bit 6 = "0": Count forwards for data transfer, i.e. lowest address first.

Bit 6 = "l": Count backwards for data transfer, i.e. highest address in buffer first.

Bit 7 = "1": The supply voltage (24V/0V) is taken from the peripheral interface of the DMA.

Bit ll= "l": If the content of the block length counter register has become null, an interrupt request is outputted to the central processing unit.

Bit 12= "1": If the value null (special character) is read during code transcription an interrupt request is outputted to the central processing unit.

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• AG X.0.7 Delete status flags and aid 2 0 X DA

Bit 7 = "1": DMA system reset.

Bit 8 = "1": The 10 us time monitoring for data transfer between the peripheral device and

the DMA is turned off.

Bit 9 = "1": Delete time error status message.

Bit 10 = "1": Delete parity error status message.

Bit 11 = "1": Delete block length counter

null status message.

Bit 12 = "1": Delete special character

status message.

9.1.2 Inter-Relationship Between the Content of the Block Length Counter and Status Register Bits 1, 2, 3, 4, 5, 6, 7, 11 and 12

Bits 2 (BU) and 5 (BLEN) are set to "1" when the block length counter is loaded.

- Final states after completion of DMA operation
 - Block length counter equals null, bit 2 (BU) and bit 5 (BLEN) deleted, all other status bits except bits 9 and 10 deleted.

The DMA input operation called up was completed correctly.

Bits 9 and 10 relate to the dynamic operating mode, i.e. they are irrelevant as far as DMA operation is concerned.

Bit 11 (BLZO) set, bit 5 (BLEN) and bit 2 (BU) deleted, block length indicator equals null, no other status bits set.

The DMA output operation called up was completed correctly.

Block length counter not equal to null, bit 5 (BLEN) not set, bit 2 (BU) set, no other status bits set.

The DMA input operation called up was completed correctly, although the end of area was not reached, i.e. the program envisaged more input characters than were provided by the peripheral device. The number of characters which were not received is present in the block length counter.

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Block length counter not equal to null, bit 5 (BLEN) not set, bit 2 (BU) not set, bit 1 (BU) set, not other status bits set.

The DMA input operation called up was completed correctly, but there was overflow. There is overflow when an input from the peripheral device transmits more characters to the DMA than was envisaged by the program. A statement of the number of extra characters which were received is present in the block counter in inverted form. The extra characters which were transmitted are lost.

Block length counter not equal to null, bit 5 (BLEN) set, bit 2 (BU) set, bit 3 or 4 (VPC or time fault) set, no other status bits set.

The DMA input or output operation called up was not completed correctly and was truncated. This was due to the parity or time fault memory.

The number of characters which are to be received or to be transmitted is present in the block length counter.

Block length counter not equal to null, bit 2 (BU) set, bit 5 (BLEN) set, bit 6 or 7 (FZDPDEA or FVPDDE) set, not other status bits set.

The DMA input or output operation called up was not completed correctly and was truncated. This was due to time faults or parity errors in the magnetic disk store.

The number of data items which are to be transmitted or received is present in the block length counter.

Block length counter not equal to null, bit 2 (BU) not set, bit 5 (BLEN) set, bit 1 (BU) set, bit 6 or 7 (FZDPDEA or FVPDDE) set, no other status bits set.

The DMA input operation called up was not completed correctly and was truncated. This was due to time errors or parity errors in the PSP. There was also overflow.

A statement of the number of extra characters received is present in the block length counter in complementary form.

Bit 9 (FZDPDY) or bit 10 (FVPDDY) set; other status bits can be set as required, since simultaneous operation is permitted between DMA operation and dynamic operation.

A time error or a parity error was detected in the PSP when a dynamic input or output instruction was made.

At the time of writing bit 12 is not used.



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Delete status bits

Delete status bits Status bits 9, 10, 11 and 12 must be deleted for each output instruction (AG 7).

Note: Bits 9 and 10 are not always reset after a fault has occurred, care must therefore be taken in the evaluation of these bits.

The other status bits are reset by the interrogation instruction EG 4.

9.2 Interrupt Release in DMA

Interrupts can be released by bit 11 (BLZO) and bit 12 (special character).

With BLZO = "1" it is therefore possible to signal the end of DMA output operation by an interrupt release (this must, however, have been determined previously by outputting bit 11 on AG 6).

At the time of writing interrupt release by means of recognition of special characters is not used.

The system is not informed of the completion of a DMA operation by the release of a DMA interrupt. If the end of an input operation is signalled by an interrupt then it is an interrupt from an external peripheral device.

9.3 DMA Addressing

The DMA address used at the time of writing is 6.0.X. X = input or output line

correctly and was trundated. This was due to time

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DMA Header 5000

The DMA feature constitutes the connection between the DMA 1804 and the tape control unit. ne tape control unit.

10.1 I/O Assignment of the Magnetic Tape Control Unit

Bit Row	8	7	ne 1	3 (d 5	4	က	2	-
EG 0.0 device information adr.	1E 8	IE 7	IE 6	<u>п</u>	1E 4	E 3	1E 2	1E 1
EG 0.1 read data	Inf. 8	Inf. 7	Inf. 6	Inf. 5	Inf. 4	Inf. 3	Inf. 2	Inf. 1
EG 0.0 + GA Status 0	ade:	19 m	191 I	ens cont	in a		NRZI/PE device	9/7 channel
EG 0.1 + GA Status 1	NA(FF)	PF(FF)	TEMP	utic ape cei	CERS (FF)	DATAER (FF)	ZTF (FF)	REJECT (FF)
EG 0.2 + GA Status 2	Hynet Stat Be i Carl	IDENTS (FF)	вот	FPT	RWD	RDY	FM (FF)	EOT (FF)
EG 0.3 + GA Status 3	id 94 9981 1 98 (39)	11 (5) 6#11	ali Ri i	enia Pacea Se es	D-BUSY	C-BUSY	3 80 Lucu	d e
AG 0.1 write data	Inf. 8	Inf. 7	Inf. 6	Inf. 5	Inf. 4	Inf. 3	Inf. 2	Inf. 1
AG 0.0 + GA device information adr.	IA 8	IA 7	146	IA 5	1A 4	IA 3	1A 2	IA1
AG 0.1 + GA	ed em 16	(6. (8)	enc	oded instruction	encoded instructions (see list of instructions)	- A	1 I	loids LE
instructions								
AG 0.2 + GA					20.20		AU	IVON.
instructions							2V LN	NOOD

GA = device address

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10.1.1 Description of I/O Assignment

There are 4 input instructions and 3 output instructions. Inputs EG 01. and output AG 0.1 relate exclusively to independent DMA transfer.

EG 0.1 = Input data characters for independent operation. AG 0.1 = Output data characters for independent operation.

10.1.1.1 Input Instructions

- Interrogate the interrupt number of the EG 0.0 magnetic tape control unit.
- EG 0.0+GA Interrogate the status bits of status line 0.
 - Bit 1
- "0" = channel 9"1" = channel 7
 - "1" = PE device

 - "0" = NRZI device
- EG 0.1+GA Interrogate the status bits of status line 1.
 - Bit 1 REJECT (FF) instruction not accepted. This state is set if an instruction from the magnetic tape control unit is not accepted.

The following conditions entail REJECT:

- The magnetic tape control unit is still working and receives a new instruction (except OST).
- Rewind instruction received when the b) device is at BOT.
- Write instruction without write entry. C)
- Invalid instruction code.

Bit 2 ZTF (FF) time error

> This state indicated that, during data transfer between the magnetic tape control unit and the magnetic tape station, information was not accepted on time by the receiver (e.g. because of incorrect start stop time).

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Bit 3 DATA ER (FF) check character error

This state indicated that an error was detected during read or check read for a write operation.

in NRZI in PE

VPC error correctable error (CERS-"1")

LPC error incorrectable error (CERS-"0")

or defective preamble or postamble skew failure or drop out on more that one track

Bit 4 CERS (FF) single error corrected

This state only applies to PE devices during read operations. It indicates that there was a single error which was automatically corrected.

A single error means that a l-bit error correction was made in a data character (bit added automatically).

Bit 6 TEMP (temperature error)

"l" = the internal temperature of the device is too high.

Although this state does not affect readiness to work it can however, lead to information errors if the device continues to be operated.

Bit 7 PF (FF) parity error

"l" = there was a parity error in the magnetic disk store in an information cycle or in a data cycle.

Bit 8 NA (FF) power failure

"l" = the power pack of the magnetic tape control unit has reported NA.

EG 0.2+GA Interrogate status bits of status line 2

Bit 1 EOT (FF) end of tape mark

"1" = end of tape mark detected.

Bit 2 FM (FF) tape mark detected.

Bit 3 RDY ready to operate

"l" = the device addressed is on REMOTE and is ready to accept an instruction.

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- Bit 4 RWD rewind status
 - "1" = the device is rewinding and has not yet reached BOT.
- FPT reel write enable ring Bit 5
- "0" = no write enable ring on rel. No write "0" = no write enable rimentry can be made.
- BOT beginning of tape mark Bit 6 "1" = the tape is at BOT.
- Bit 7 IDENTS (FF) PE indentification block detected.
- "l" = PE identification block detected during the first read instruction (first time tape is addressed). The tape in question has already been written on by the PE.
 - Interrogate the status bits of status line 3. EG 0.2+GA
 - Bit 3 CBUSY magnetic tape control unit activated.
 - "1" = an instruction is being dealt with in tosses to see the magnetic tape control unit.
 - Bit 4 DBUSY write or read status
- "1" = the magnetic tape control unit is dealing with the part of an instruction sequence in which data is being written or being read. disk store in an information oxcle or

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10.1.1.2 Output Instructions

- Load the interrupt register of the magnetic AG 0.0+GA tape control unit (the interrupt number must be in bits 1 to 4).
- AG 0.1+GA Output encoded magnetic tape control unit instructions.

List of instructions for the magnetic tape control unit.

Abbreviation	Description	Code
DBS	Write a data block	4.1
DBLV	Read a data block forwards	2.1
DBLR	Read a data block backwards	2.2
BS	Write a tape mark	4.2
DBV	Unwind one data block	2.7
DBR	Rewind one data block	1.1
GV	Run forward 64 mm with erase	4.4
RW	Rewind to beginning of tape	
	mark	1.2
RWL	Rewind to beginning of tape	
	mark and switch off	1.4
LV	Changeover read threshold	0.3
UP	Changeover parity bits	1.7
DDS	Changeover bit density	2.4
OST	Stop operation	0.0

- AG 0.2+GA Output for interrupt inhibit or interrupt enable.
 - Bit 1 TVSN

Implement interrupt lock.

Bit 2 IVLN

Delete interrupt lock.

10.2 Interrupt Release

Each instruction, except "rewind" and "rewind and switch off", is terminated by an interrupt.

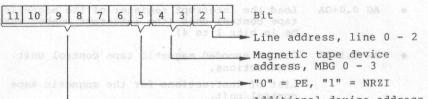
The interrupt line can be disabled or enabled by means of the instructions "set interrupt lock" (IVLN) and "reset interrupt lock" (IVLN).

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Read a data block ferwards Read a data block backwards



Additional device address (coding connector in magnetic tape control unit)

BS DBV DBR GV GV RW

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11 DMA Header 0411.01 transplace A Out to maintain seed to 1.1.11

The DMA feature connects the DMA 1804 and card reader 0491.01 or 0492.01.

11.1 I/O Header Assignment

Row Bit 8	EG 0.0	EG X.V.1 parity error	EG X.Y.2	EG X.Y.3 timing	EG X.Y.4 counter 0	EG 0.1	AG X.Y.0	AG X.Y.1 0 -	AG X.Y.2	AG X.Y.3 0	-
7		multi- punching	aul i	Busy	3W0 C	6 N	ed be	3110	5. B		- Parel
9	63 J	ERROR	informa	row 3	row 9	inform	interri	Care Cann	K=last	= ast	a de con a la com
S	interrupt address	HOPPER	tion from chanr	row 2	row 8	nation from cha	interrupt address —	nber of columns	K=last column before window	l =last column of a window	1
4	dress	MOTION	information from channel amplifier via DMA to CPU	row 1	row 7	information from channel ampliefier to the DMA	30 3 5 21 128	L=number of columns to be transmitted	window	wopu	40101
e	*Sas aqas d st	READY	DMA to CPU —	row 0	row 6	to the DMA	315 081 8-1-8	Pe	T 1 8 4		+11000
2		start read cycle	ands	row 11	row 5	33 4 33 83 140 8	i Di	7 9 F0	1 2	£ . 3	4
9 - 1	ol s ni ba t	488 CPO 24 b	adin adi	row 12	row 4	ili di d	ogni iv (tel	sid ella ensi	T d		interrint

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11.1.1 Description of I/O Assignment

There are 5 input instructions and 5 output instructions.

11.1.1.1 Input Instructions

- EG 0.0.0 This is an instruction to interrogate the interrupt number of the feature.
- EG 0.1 This input line transmits data located in the buffer via the DMA to the CPU (independent transfer). This line cannot be addressed via dynamic instructions.
- EG X.Y.1 Interrogate reader status bits
 - Bit 2

 This bit is set when "start read" is outputted. It is deleted by the dynamic input instruction EG X.Y.1, after the end of data transmission interrupt, by a power failure in the card reader or by outputting "clear buffer". If the flag is deleted because of a power failure, the last card transported must be replaced.
 - Bit 3 READY

This bit indicates that the card reader is ready to operate and respond to a card transport instruction. This bit is reset by a power failure or a fault in the card reader.

Bit 4 MOTION CHECK

This bit indicates a transport fault. Either card n could not be transported or card (n-1) could not be stacked properly. This signal is cleared by a power failure.

Bit 5 HOPPER CHECK

This bit either indicates that the hopper is empty or the stacker is full. Do not replace any cards.

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Bit 6 ERROR

This bit is set if an error is detected at the beginning and the end of a card when it is being read during light/dark checking. The card in question must be replaced and read again.

This signal is cleared by a power failure.

Bit 7 Multi-punching

This bit is set if more than one hole is detected in rows 1 to 7 of a column of a card. The setting of this marker is suppressed during binary data transmission and for a single window mask. This flag is deleted by the next dynamic EG X.Y.l instruction or by a power failure.

Bit 8 Interface parity error

The "parity error" flag is set if, during transmission from the DMA to the card reader DMA feature, a parity error is detected in an information cycle. In addition the signal QUITT (acknowledge) is not switched. The DMA will therefore detect a time fault. If a parity error is detected in an address cycle only the QUITT (acknowledge) signal is not switched.

• EG X.Y.2 Information from a card which has been read is present in the DMA feature buffer and can be read into the CPU dynamically via the DMA. In this case no interrupt is released for the end of data transmission. It is also possible to initially transmit a few columns dynamically and transmit the remainder by independent data transfer.

• EG X.Y
3 and 4 The 12 information lines of the card reader can be interrogated by means of input lines
3 and 4 (bits 1 to 6).

Bit 7
on EG 3 This bit denotes the state of the card reader
BUSY signal.

Bit 8
on EG 3 This bit changes its state from index mark to index mark when a card is being read.

on EG 4 Column counter

Bit 8 is set when the card reader DMA feature column counter is null.

Bit 8

11.1.1.2 Output Instructions

- AG X.Y.O Load the interrupt register of the DMA feature (the interrupt number must be in bits 1 to 4).
- AG X.Y.1 Output the number of columns to be transmitted from the DMA feature buffer to the CPU.
- AG X.Y The location of a window which is to be blanked 2 and 3 (e.g. microfilm window) can be defined by the following outputs:

AG 2: K = last column before the window

AG 3: I = last column of the window with K not greater that 80 and I not greater than 80.

- AG X.Y.4 Output the operating mode bits
- Bit 1 Interrupt channel inhibit

The release of interrupts by the card reader DMA feature can be inhibited by outputting bit 1 = "1". All other functions remain unaffected.

Bit 2 Start read

Outputting this bit initiates the reading of a card, provided that the card reader is in the READY operating state. Card information is transmitted to the header buffer. "Start read" for the next card does not occur until the "end of read" interrupt has been processed.

Bit 3 Start transmission

When this bit is outputted the card reader DMA feature starts automatic data transmission with the DMA. The specified number of column information items (output on AG 1) is transmitted to the CPU.

Bit 4 Clear instructions

The contents of the buffer is invalidated when this bit is outputted. The flag multi-punching, start, read cycle, read timing, interrupt inhibit, parity error information, column counter, window registers and FF interrupt flags are cleared and reset. A new read cycle can now be started.

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Bit 5 Binary data transmission

Data is transmitted in binary form when this bit is outputted. Data is transmitted in encoded form when this bit is not set.

Standard punched card, encoded

This operating mode is the most widely used. The information for one column is transmitted in 8 bits = 1 byte.

Lines 1 to 7 are encoded in binary form in bit 3, whilst the remaining 5 lines are outputted directly.

 $\begin{bmatrix} 20\\21\\22\\3 \end{bmatrix}$ Lines 1 to 7 encoded Bit 1: Bit 2:

Bit 3: Bit 4: Line 0

Bit 5: Line 11 Bit 6: Line 12

Bit 7: Line 9 what such to bee edd is to

Bit 8: Line 80 need and sleidnl squiresmi

Standard punched card, binary

This operating mode is selected by setting bit 5 in output line 4. Each column is transmitted in two bytes. The flag "multi-punching" cannot be set.

Bit assignment for the two bytes:

Byte 1		Byte 2			
Bit 1: Lin	e 12	Bit 1:	Line	4	
Bit 2: Lin	e 11	Bit 2:	Line	5	
Bit 3: Lin	e 0	Bit 3:	Line	6	
Bit 4: Lin	e 1	Bit 4:	Line	7	
Bit 5: Lin	e 2	Bit 5:	Line	8	
Bit 6: Lin	e 3	Bit 6:	Line	9	
Bit 7: 0		Bit 7:	0		
Bit 8: 0		Bit 8:	0		

Read marked cards Bit 6

This bit must be outputted either before or at the same time that the instruction "start read" is outputted in order to inform the card reader DMA feature that marked cards are to be read. In this case the "end of read" interrupt is not requested immediately after the last index mark but 40 us max. after the card reader signal BUSY becomes "0". The maximum read speed of the card reader is also reduced.

Bit 7 Check interrupt and Visalia 2 dis

When this bit is outputted the card reader DMA feature requests an interrupt (in order to check the interrupt circuit).

Bit 8 Pick command

When this bit is outputted the transport of a card is triggered. Other functions of the card reader DMA feature remain unaffected.

All the bits of the output line 4 reset internally, with the exception of bit 1. Bit 1 can only be reset by the program.

11.2 Interrupt Release

An interrupt can be released either at the "end of read cycle" or at the "end of data transmission", provided that the interrupt inhibit has been cancelled.

11.3 Addressing

The address X.7.n is used at the time of writing.

sional 9957 percent "0", The maximum read aread

X = DMA 1804 address = 6.0.0

n = Line address

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12 Printer DMA Feature 4600

The printer DMA feature connects the DMA 1804 and the printer.

12.1 I/O DMA Feature Assignment

	Bit 8	c be	9	16.	#43#0 # 8# # 6 1 8	e e	196 a 1991 1991 1991	
, A	check	automatic	Inf.	end of	od of buffer	13 T B	indicator	end of
			Parity		combos			i
EG X.Y.2	parity	automatic	03 3	o a lo	printer identification		a n ton ton ton ton	- 04 C
EG X.Y.3	Page	Load	Parity	. peej	end of form	end of paper	indicator	printer
AG X.Y.0	Seel	Bud an T		interrupt number	t number	teres	9959 964 9708 88 7	guan
AG X.Y.1	check interrupt	automatic ready	Inf. Parity	end of feed	buffer empty	663 586	indicator	end of print
AG X.Y.2	0	0	0	n. isni	0	operati	operating char. *	5 d :
AG X.Y.3		AMD into the bes	yd is od s	characters to buffer	ler -	teet beet	tigger tigger a light	efe o es
AG X.Y.4		end o m d de	19 31 (3qe) (80)	-characters to printer	iter	ekog V ad Eg ik	10001 11 301 1000 11 901	11 d 1
AG X.Y.5	n a lola la la la la la la	0843 13100 1001	ed l	-characters for automatic	tomatic ———	line Liso Lad d	11 A1 12 31 13 30 15 A1	etal Sest
AG X,Y.6				- number for automatic	natic			
Code	* Code Function	1887	b	O S	Code Function	200		1.7.8
5 - 0	Clear header buffer Start DMA transmission Start transmission from DMA feature	r buffer transmission ission from	DMA fea	3 ture 5	Release check inter Delete parity error Clear DMA feature	Release check interrupt Delete parity error Clear DMA feature	-bt	08 e

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widerhand ungen in der Penatierfilig oder Getraufstansser-Einfanne vorheralen.

12.1.1 Description of I/O Assignment

There are 4 input instructions and 7 output instructions.

12.1.1.1 Input Instructions

- EG 0.0.0 Interrogate the interrupt number of the line printer DMA feature.
- EG X.Y.1 Interrogate the interrupt cause bits.

The 8 bits of this line indicate the reason an interrupt was released. This line is deleted as soon as the input instruction has been performed, and can therefore only be interrogated once for each interrupt from the line printer DMA feature. Interrogation can also be used to reset the markers.

Bit 1 End of print

The end of print interrupt is always generated when the printer transmits its request signal and is ready to accept new characters as well as when the indicator is reset by the outputting of an end character.

Bit 2 Indicator

The indicator interrupt is switched by the indicator signal from the printer (see status bit indicator).

Bit 4 Buffer empty

The empty buffer interrupt is released when the independent transmission of characters from the DMA feature buffer to the hardware buffer of the printer has been completed.

Bit 5 End of feed

The end of feed interrupt is released when the printer rejects the feed signal.

Bit 6 Information parity

This interrupt is released when a parity error occurs in the PSP during block transmission.

The line printer DMA feature truncates block transmission and the DMA indicates a time error.

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Bit 7 Automatic ready

The automatic ready interrupt is released when the automatic entry of characters (e.g. enter X blanks in the DMA feature buffer) has been completed.

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This interrupt can be used to check the interrupt circuit and has no other significance of function.

• EG X.Y.2 Interrogate printer identification and the status messages of the character printer DMA feature.

Bits 1 to 6

Printer identification

Bit 8 Check interrupt

These bits provide information concerning the wiring of the coding connector of the printer and enable the program to determine the type of printer (300, 600, or 1200 lines) and the character configuration of the print drum or print chain in question.

Possible printer identification:

0.0 or 0.2 Print mechanism with normal drum
0.3 Print mechanism with dual numerical drum

Bit 7 Automatic active Paibnavks

This bit is set whilst the internal automatic equipment of the DMA feature is running. Since automatic operation is very rapid and the bit is present for a correspondingly short period of time, recognition is only possible from approximately 20 characters up.

Bit 8 Parity error

This bit is set when an information parity error (hardware fault in the PSP) occurs during dynamic output instructions. This flag is deleted by the instruction "delete parity error".

• EG X.Y.3 Interrogate printer status bits

Bit 1 Request was said and

The printer is ready to accept characters in its hardware buffer. When "request" is switched, indicator, end of paper and internal parity must not be set.

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Bit 2 Indicator

The printer is not ready to operate because:

 a) An illegal character or a character with incorrect parity was outputted.

In the following cases "indicator" can be deleted by the outputting of the end character. The printer is not triggered.

- b) The paper has run out of the upper tractor and the printer is printing without paper.
- c) The print member is swung off.
- d) The channel tape reader is open.
- e) A parity error has occurred in the hardware buffer of the printer.

Bit 3 End of paper

End of paper under the lower tractor.

Bit 4 End of form

Channel 12 on the channel tape has been detected. The flag is reset by the next end character that triggers a print.

Bit 5 Paper advancing

This bit is present as long as the paper is advancing.

Bit 6 Internal parity

A parity error has occurred in the hardware buffer of the printer. The indicator is set simultaneously. This flag can only be reset if the red reset button on the printer power pack is depressed or by switching the printer off and on. In this case wait approx. 10 seconds until the capacitors in the power pack have discharged.

CAUTION: The line printer DMA feature must subsequently be initialized once more.

Bit 7 Load image

This bit can only be set when using the chain printer, when the latter demands the image of the chain after switching on.

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Bit 8 Page mont molecularing

Not used at time of writing.

12.1.1.2 Output Instructions

AG X.Y.O Load interrupt number (the interrupt number is in bits 1 to 4).

The interrupt number is used to identify the device which is requesting the interrupt and is transmitted when the CPU is giving an EG 0.0.0 instruction and the DMA feature has interrupt priority.

AG X.Y.1 Enable interrupt conditions

"O" = Enable "l" = Disable

All interrupts are disabled by switching-on clear, adapter clear or by depressing the red reset button on the printer power pack.

Output the operating characters AG X.Y.2

Code 0 Clear DMA feature buffer

The internal buffer address pointer is set to zero, i.e. the data which now follows will be placed in the buffer from address "null" onwards and, when printed, will therefore appear on the paper from position "null" onwards. Thus a new line is started.

Start DMA transmission Code 1

The DMA must be prepared before this instruction is outputted i.e. the block length counter and the block address counter must be loaded.

If a hardware parity error occurs in the PSP during block transmission, the line printer DMA feature truncates data transmission and releases an information parity interrupt. The DMA indicates a time error.

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Code 2 Start transmission from line printer DMA feature to the printer.

This instruction transmits the content of the DMA feature buffer to the hardware buffer of the printer. Only as many characters as were written into the DMA feature buffer after the last "clear DMA feature buffer" instruction are transmitted. The end of the transmission is reported by the "buffer empty". If the instruction "start transmission from the line printer DMA feature to the printer" is outputted again after a print operation has been performed, transmission takes place again. The contents of the DMA feature buffer is retained until it is written over. Duration of transmission: 1.6 us per character.

Code 3 Release check interrupt

This instruction releases an interrupt. It has no further effect.

Code 4 Reset parity error flag

This instruction resets bit 8 in line 2 which is set by parity errors during dynamic output instructions.

Code 5 Clear DMA feature

The line printer DMA feature acknowledges this instruction and clears itself, i.e. all registers are set to "null" and all interrupts are inhibited (as is the case after CPU deletion or switching on).

AG X.Y.3 Output character to the header buffer.

This instruction writes the character located in the A register of the CPU into the DMA feature buffer after the characters already located in the DMA feature buffer. No check is made to determine whether the character is legal for printing purposes.

AG X.Y.4 Output character to the printer buffer

This instruction writes in the character located in the A register of the CPU directly into the hardware buffer of the printer. The DMA and the line printer DMA feature function as normal I/O: The acceptance timing bit for the printer is formed by the line printer DMA feature hardware. The control characters for print release 0.12.2 (end character), for line feed 0.4.0 and channel feed 0.12.1 are also outputted on this line.



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• AG X.Y.5 Output a character for the DMA feature register.

This instruction loads a register in the line printer DMA feature with a character that is to be written into the DMA feature buffer automatically. This character remains in the register until it is written over.

 Ag X.Y.6 Output the number of characters for the DMA feature register.

This instruction loads a counter in the line printer DMA feature and immediately writes in the inputted number of the loaded character into the DMA feature buffer with "character for automatic". The end message is by means of the "automatic operation ready interrupt". The number of characters can be between 0 and 255. (There is also an interrupt for the number "0").

The instruction "start DMA" can be outputted even when an automatic operation is running. There is a lag and the line printer DMA feature starts the DMA as soon as the automatic is ready, provided that the DMA was prepared and the automatic ready interrupt is inhibited.

12.2 Interrupt Release While Operating the Printer

The end of each operational stage (automatic ready, end of transmission to the header buffer, end of transmission to the printer buffer, buffer empty, and end of print) is reported by an interrupt.

12.3 Addressing

The address X.6.n is used at the time of writing.

X = DMA address = 6.0.0

n = Line



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13 1/0 1806

The I/O 1806 is used to control the line (V24 interface).

13.1 I/O Assignment

Bit D L Row 3 2	EC V 1		EG Y.2 0 1	EG Y.3 0 1	EG Y.4 3 1 1	EG 0.0.0 0 0	AG Y.1 0 0	AG Y.2 0 1	AG Y.3 0 1	AG Y.4 1 0	AG Y.5 1 0	2 2 2 2	-	AG 7 (Y0) 0 0	AG 8 (Y.0) 0 C A9.11=0 0 C	AG 9 (Y.0) A9 . 10 = 0
2 1	-	-	0	-	-	0	0	1 0	13 110	0	0	-		0	0 0	0 0
ed 8	ne.	0	35.0	autom, call — modem —	a w	338	7911 1985	eq ea a	8,0	autom, call=1 modem = 0	-			2.3	18	
7 %	63 03	90	read shift chain empty	# # HEO 7: 1 3 9	shift chain empty	tea he id laupi	i (1) (2) (2)	614 5eg 15res	changeover timing ——	I/O test connection D1 to D2	ed om ob				shift chain empty	
9			receiver buffer full	4 1	receiver buffer full	1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	ool bevi link	y er	uor eu	dual stop element	8			E 3	receiver buffer full	
s S	input buffer		send buffer free	M 24 station disconnected	interrupt request	interrupt address-	send buffer —	- synchronous cl	signal ne- gation D1 and D2	character length 5 to 8 bit	id id			interrupt address	interrupt inhibit send buffer	addr
4	9.0		status interrogation	M 25 power indication	equest M5	SS	W 24	synchronous character buffer	53 5	length	reset sync FF and receiver	-	S 4	address	W2	address preselection
£	80		Break	M 23 abandon call	M3	0100 2005 2005 2005 (1005)	-digit bits for autom. calling – W 23 W 22	lett Lept sept	timing rate	ODD = 1 EVEN = 0	reset interrupt request and buffer	S22 digit present	83		ε Σ	
2	0 E	7 4 5 0	parity error	M 22 present next digit	M2	Gudi Gudi Gudi	om. calling — W 22	noit noit s s	bed: lago lago	parity generation	Reset Parity Lost Data Break	S21 call request	52		M 2	
les lij	va a	5 8 8 8	Lost	M 21 data line occupied	-	្រាស់ ទោកវិ ទោកវិ	W 21	3 8: 50 :	high speed = 1 slow = 0	sync = 1 async = 0	Master Reset Sender	and State	S 1 Modem		2	*

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13.1.1 Description of I/O Assignment

5 input instructions and 9 output instructions are required to control the line.

13.1.1.1 Input Instructions

 EG X.Y.1 Interrogate the data input buffer (receiver buffer)

The buffer can be interrogated at any time required, except in the synchronous operating mode and when synchronization has not been completed.

Interrogation of the buffer triggers the deletion of the "buffer full" message.

If the buffer is reloaded during the strobe signal EG 1, an incorrect information item can be accepted. This results in the error message "lost data".

- EG X.Y.2 Interrogate status bits
 - Bit 1 Lost data

If strobe signal EG 1 is detected before the transfer of a new data item into the input buffer, the error flag is set.

Bit 2 Parity error

If a parity error is detected when serial data is being received a flag is set (pay special attention to parity).

Bit 3 Break error message

This error flag is set if a format fault has been detected in the synchronous operating mode (incorrect sequence: start, 5 to 8 bits, data, stop).

Lost data, parity error and break can be reset by means of reset 2.

- Bit 4 Not used
- Bit 5 Send buffer free

This bit is "l" when the send buffer is ready to accept new information.

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Receiver buffer full Bit 6

This status bit is equal to "l" if there is a character in the input buffer which has not been processed. This bit is not affected by lost dat.

Bit 7 Send shift chain empty

> This status bit is equal to "1" when the send buffer and the shift chain are empty. The message "shift chain empty" only goes to "1" when a transmission has been made i.e. the message "shift chain empty" is not reported immediately after switching on or immediately after master reset sender (AG 5).

A tape card reader message is cleared by master reset sender (AG 5) or by AG 1 (load send buffer).

Bit 8

not used it is and isvissed in

EG X.Y.3 Interrogate message signal

This line contains status messages from data communication equipment or from the special sub-assembly for automatic dialling.

Bit 8 = "1": Messages from the AWD

Bit 8 = "0": Messages from data communication equipment equipment

Bit	Data communication equipment	AWD 0 0 08
1	Ml data set ready	M21 data line occupied
2	M2 ready for sending	M22 present next digit
-3	M3 calling indicator	M23 abandon call
4	M5 data carrier detector	M25 power indicator
5		M24 distant station connected

Interrogate interrupt request flags EG X.Y.4

Bit 1

M1

This bit is set if a change in the interface signal Ml is detected.

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0 0 0 0 0

nder Satt

Bit 2

M2 The relied reviews 3 318

This bit is set if a change in the interface

signal M2 is detected.

Bit 3 M3

This bit is set if a change in the interface

signal M3 from off to on is detected.

Bit 4 The or M5 lade dilde and bas islind MIT of sace vice

This bit is set if a change in the interface

signal M5 is detected.

Send buffer free Bit 5

This bit is set if a character which has been loaded in the send buffer is accepted into

the shift again (send buffer free).

Receiver buffer full Bit 6

This bit is set if there is a valid character

in the receiver buffer.

Bit 7 Shift chain empty

This bit is set after a master reset sender (bit 1, AG 5) or NLO when the send buffer

has been loaded at least once and the character has been transmitted in its entirety to the

data communication equipment.

EG 0.0.0

Interrogate interrupt

This line is used, after an interrupt from the system, to interrogate the interrupt address

of the I/O which requested the interrupt.

The interrupt number is in bits 1 to 8.

M5 data cartier

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13.1.1.2 Output Instructions 13 and probably and 198

• AG X.Y.1 Load send buffer

Bits

1 to 8 Information to be outputted

Bits 1 to 4

Dial bits for automatic selection.

Dialling information is set out in accordance with the code table below.

Dial bit	4	3	2	1
Switched connection	W24	W23	W22	W21
Dial signal	Bi	t com	binat	ion
and the state of t	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	-1	0	0
5	0	-1	0	1
6	0	more made	1	0
7	0	1	1	1
8	-1-	0	0	0
9	1	0	0	1
0	0	0	0	0
EON	1	1	0	0
SEP	1	1	0	1

The character EON (end of number) identifies the end of the dial signal sequence and prepares the data communication equipment to receive a signal from the called station (e.g. answering tone) to acknowledge establishment of connection.

The character SEP (separation) can be inserted in the sequence of dialling digits and enables the automatic dialling equipment to comply with the pauses during the dialling process which are imposed by certain trunk networks.

The signal status of lines W21 to W24 must not change as long as line S22 "digit present" (AG 6) is switched on.

• AG X.Y.2 Load the sync character buffer

Bits 1 to 8

Bits 1 to 8 contain the code of the sync character. The sync character buffer is required in order to compare the sync characters.

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AG X.Y.3 Set the timing rate, timing transition (external, internal) and signal inversion of Dl and D2.

Bits 1 to 4

Output timing rate

Rate (Baud)	Bit 4	Bit 3	Bit 2	Bit 1
9600	0	10 010	0	0
7200	0	0	1	0
4800	0	0	0	1
3600	0	0	1	1
2400	0	1	0	0
1800	0	1	1	0
1200	0	1	0	1
900	0	1	1	1
600	1	0	0	0
300	1	0	0	1
200	1	0	1	0
150	1	1	0	0
100	1	1	1	0
7 5	1	1	0	1
50	1	1	1	1

Bit 5

Inversion bit for control signals D1 and D2 of the V24 interface.

Bit 5 = "0": D1 and D2, positive voltage Bit 5 = "1": D1 and D2, negative voltage

Timing switching for different operating modes

O	perating mode	Bit 6	Bit 7	Bit 8
	Internal send and receiver timing	T ado edi ado the	0	0
2	External send and receiver timing	0	0	1
3	Internal send timing and external receiver timing	ple eff eprad (2 08)	1 ,	0
4	External send timing and internal receiver timing	0	1 ₅ y.	x 2A 0

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• AG X.Y.4 Load the operating mode register

Bit 1 Bit 1 = "1": Switch the I/O to synchronous

operating mode.
Character format without start

values of the bas surger and or stop element.

Bit 1 = "0": Switch the I/O to asynchronous

operating mode.

Effect: Character format in start and

stop bit.

Synchronization starts with the start bit.

Bit 2 Parity generation

Bit 2 = "1": Transmitted data is automatically supplemented with on ODD or EVEN parity bit, depending upon how bit 3 is set.

The bit with the highest value character length is replaced by the parity bit which is formed.

Bit 3 ODD/EVEN parity switching

Bit 3 = "1": Transmitted data is supplemented with an ODD parity bit (if Bit 2 = "1") and received data is checked to ensure that it is odd.

Bit 3 = "0": Transmitted data is supplemented with an EVEN parity bit (if Bit 2 = "1") and received data is made EVEN.

Bit 2 is set in EG 2 if the parity of the characters which are received differs from the parity which has been set.

Bit 4 + 5 Definition of character length

Bit 5	Bit 4	Character	length	(bit)
0	0	5		
0	1	6		
1	0	7		
1	1	8		

Note: The parity bit which is generated is included in the length of the character.

Bit 6 Definition of the stop element

oter Ger

Bit 7 Switching the I/O to the test operating mode

Bit 3 = "l": Transmitted data Dl is linked internally with the received data.

The voltage level of the line D1 at the modem interface remains negative and the receiver is inhibited for received data from line D2.

Bit 8 Switching to automatic calling and modem operating mode

Previously set modem conditions are retained.

AG X.Y.5 Output reset conditions

Bit 1 Reset sender

This resets the sender system before a transmission.

Bit 2 Reset parity, lost data and break

This bit resets the parity error, lost data and break status messages of input line 2.

Bit 3 Reset interrupt request and interrupt buffer
This bit can be used to reset the interrupt
request register and the interrupt buffer.

Bit 4 Reset receiver and sync flip-flop

This bit is used to reset the receiver system for the reception of data. Ensure that the operating mode register is not affected by this system reset.

In the synchronous operating mode this reset necessitates character synchronization once more.

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• AG X.Y.6 Set the connected data communication equipment

This line can be used to drive data
communication equipment. This is the case in

the modem operating mode with S1 to S4 and for automatic dialling with S21 and S22.

Control signal S3 is not used in the I/O 1806 at the time of writing.

Switching from the modem operating mode to automatic dialling and vice versa does not affect previously set control lines. The register is set to "0" by NLO after switching on and the voltage level of the control lines at the V24 interface becomes negative (off state).

• AG X.Y.0 Corresponds to AG 7 in the I/O assignment (AG 7) when bits 9 to 12 of the output information are "null"-

Load the 8-bit interrupt register of the 1806.

• AG X.Y.O Corresponds to AG 8 in the I/O assignment when (AG 8) bits 9 to 11 = "0" and bit 12 = "1" in the output information.

Set or reset the interrupt inhibit bits.

Interrupt inhibit = "1": The corresponding channel is inhibited.

All channels are inhibited after switching on.

AG X.Y.0 Corresponds to AG 9 in the I/O assignment when (AG 9) bits 9 and 10 = "0", bit 11 = "1" and bit 12 = "0".

An address preselection is performed.

The number of the I/O 1806 to be preselected is in bits 1 to 8. Preselection remains valid until the next address preselection.

13.2 Interrupt Release

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The communication of the I/O is interrupt-controlled. See interrupt release by means of interrupt request bits on EG 3.

13.3 Addressing number at ab freshedron and sea 2.4. X 24.

The I/O is addressed by preselection (output instruction AG 9) and by means of the PSP address.

Preselection is necessary since it is possible that there can be several I/O cards in the system and these I/O cards can be addressed via the same PSP address (1.F.O at the time of writing).

Li	ne	sperat	Address	Preselection
1.	Trunk	line	1.F.0	0.0
2.	Trunk	line	1.F.0	0.1
3.	Trunk	line	1.F.0	0.2
4.	Trunk	line	1.F.O.	0.3
5.	Trunk	line	1.F.0	0.4
6.	Trunk	line	1.F.O	0.5

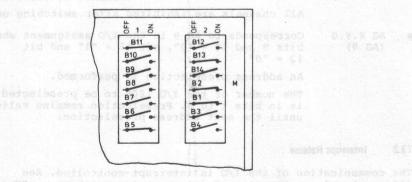
13.4 Interface Wiring

Various V24 interface circuits (coding switches) can be used so that the I/O can be connected to various data communication equipment.

The V24 interface can be modified by changing the switch positions of the two built-in 7-pin AMP switches in order to drive various data communication equipment.

The switches are located on the component side of the I/O at IC positions M1 and M2.

Coding switches (DIL switch)



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Int	erface signal	Example of application	Sw	ritch
	From the data trans-	normal	В	6
		connected to node 0513		
	From the data trans- mission unit	normal		8
M2	set at +12V			
		connected to node 0513	-	STATE OF THE PARTY OF
	From the data trans-	ta trans- t e.g. modem connected to node 0513 B ta trans- t connected to node 0513 B ta trans- normal B for installations without remote connection (e.g.,900Ml) ta trans- normal B for direct connection where required by operating full duplex data trans- mission unit and line wiring e.g. connected to node 0513 B high speed data transfer rate with D 1200 S =	10	
M3			100	9
	From the data trans- mission unit set at +12V connected to node 0513 B from the data trans- mission unit set at +12V connected to node 0513 B from the data trans- mission unit set at +12V connected to node 0513 B from the data trans- mission unit set at +12V for installations without remote connection (e.g.900M1) From the data trans- mission unit set at +12V for direct connection where required controlled by operating program set at +12V full duplex data trans- mission unit and line wiring e.g. connected to node 0513 B for installations without remote connection (e.g.900M1) From the data trans- mission unit set at +12V for direct connection where required B full duplex data trans- mission unit and line wiring e.g. connected to node 0513 B for direct connection where required set at +12V full duplex data trans- mission unit and line wiring e.g. connected to node 0513 B for direct connection where required full duplex data trans- mission unit and line wiring e.g. connected to node 0513 B for direct connection where required full duplex data trans- mission unit and line wiring e.g. connected to node 0513 B for direct connection where required full duplex data trans- mission unit and line wiring e.g. connected to node 0513 B for direct connection where required full duplex data trans- mission unit and line wiring e.g. connected to node 0513 B for direct connection where required full duplex data trans- mission unit and line wiring for direct connection where required full duplex data trans- mission unit and line wiring for direct connection where required for direct connection where required for direct connection for direct co	-		
	From the data trans-		В	13
M5	set at +12V		В	12
	Controlled by operating		В	1
S2	set at +12V	mission unit and line wiring	В	
	Routed to M2	e.g. connected to node 0513	В	2
	Controlled by operating	Celling Indicator	В	4
	set at +12V	rate with D 1200 S =	В	3

13.5 V24 Interface Wiring with SC and SD Connector

(In accordance with DIN standard 66020 and CCITT standard)

If the voltage level of a signal on a data line with respect to line E2 (signal ground) or the voltage level of a signal on a select line with respect to line E22 (ground signal) differs from 0 volt and is

- a) negative, the signal state is "l",
- b) positive, the signal state is "0".

The signal state is indeterminate in the transitional range between +3V to -3V.

If the voltage level of a signal on a control line or on a message line differs by more than 5 volts with respect to the relevant "signal ground" line, and is

- a) negative, the line is quiescent,
- b) positive, the line is in the on condition.

The signal state is indeterminate in the transitional range between +3V to -3V.

If the voltage level of a signal on a timing line differs by more than 3 volts with respect to line E2 (signal ground) and is

- b) positive, the line is in the on condition.
- Summary of Interface Lines

	Interface line	Designation DIN 66020	n to and CCITT		
7	Protective ground	- E 1	101	1 1	Γ
-	Signal ground	- E 2	1	7 	
-	— Transmitted data —	- D 1	103	2	
-	Received data	- D 2	104	3 —	
	Connect data set to line S 1.1	-S 1	108	a 200 cM	
	S 1.2 DTE ready	- Committee of the second contract of the second		20 -	
-	Request to send		105	4	
-	— Data signalling rate selector —	- S 4	111	23	
-	Data set ready — Data set ready	- M 1	107		
-	Ready for sending	- M 2	106	5	
-	Calling indicator	- M 3	125	22	
-	Data carrier detector —	- M 5	109	8 -	
-	—— Transmitter signal timing to the data transmission unit—	- T 1	113	24 -	
-	 Transmitter signal timing from the data transmission — 				
100	Receiver signal element timing from the DTU	- T 4	115	17	
land (3c confilector)	Cable 0412				
3	Protective ground	- E21	212	<u> 1 81 </u>	
3	—— Signal ground ————————————————————————————————————		201		
	—— Digit signal 20 ———————————————————————————————————			14 -	
-	— Digit signal 2 ¹ ————————————————————————————————————	- W22	207	15 -	
-	— Digit signal 2 ² ———	- W23	208	16 -	
	— Digit signal 2 ³	- W24	209	17 -	
	— Call request —	- S 21	202	4 -	
-	— Digit present —	- S 22	211	2 -	
L	— Data line occupied —	- M21	203	22	
-		- M22	210	5	
L		- M23	205	3	
L	Distant station connected	- M24	204	13	
		- M25	213	6 —	

Cable 0412



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Example of interface wiring (DIL switch)

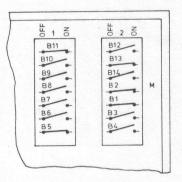
Data communication with a long distance line is via node 0513.

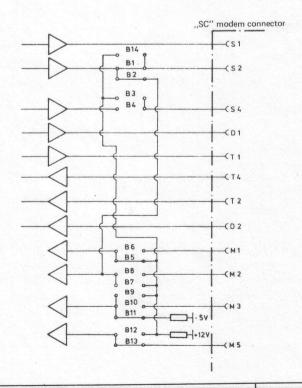
S2 (Request to send) is taken through and looped back to M2 (ready for sending) (B1, B2).

Ml (Data set ready) is set at +12V (b5).

M3 (Calling indicator for remote switching) is set at -5V (Bll).

M5 (Data carrier detector) is taken through (B13).





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For notes



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A – Pointer indicator
D – Display
T – Keyboard



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14 DTEA 1813

The I/O is used to control display 0608.01 and keyboard 0687.00 or 0687.02 via the PSP.

14.1 I/O Assignment

				3		3	U . S		93	S DO .		8.2		0.0									
	1311	input interrupt number	input interrupt number	input information	status input	input individual characters	status input	input picture refresh memory	output indicator	status output	193) 193) 193 1	output operational status	output Y cursor	output X cursor	DS DS DS								
0/1	device) O	1 M	r nij	F lugg	uo l	٥	۵	4	110	F all	۵	۵	۵	۵								
\$ 10 min	-	0	0	1	٥	ETB0	Lo	0321	LED 1	LOB	8	LOB											
	2	ola alon	a a s	u u go t lac	P F S	ETB1	PFS	A nd	LED 2	MLO	S. 3	MLO	>										
	ы	- le	io d		enI	bel	esi	ani	, LD	ETB2	0	15	LED 3	×		BS	Cursor Y						
sycle	4	I I	pt numb	pt numk	interrupt number	pt numk	pt numb	pt numb	pt numk	pt numk	- char, code	- char. code	0	ETB3	0	882	LED 4	×	- free -	×		×	char. code
Information cycle	2	interru	interru	char. c	char. c	char. c	char. c	char, c	char, c	- char. c			0	ET84	×	char, code	LED 5	×	I i	SS	×	Cursor X	- char.
Inform	9	(3 p)	n n	Je Sess	0	0	×	- char	yellow lamp	×		ō	×										
	7	0	0	o ig	0	0	×		red	×		SU	×										
16	80	0	0	OB	LN.	0	igsu ×	o lys	240 ms adder	INT	ei 4	×	×	×									
mg /	I/O Instr.	EG 0.0	EG Y.0	EG Y.1	EG Y.2	EG Y.3	EG Y.4	EG Y.7	AG Y.1	AG Y.2	AG Y.3	AG Y.4	AG Y.5	AG Y.6	AG Y.7								



14.1.1 Description of I/O Assignment

Seven input instructions and seven output instructions are required to control the display and the keyboard.

14.1.1.1 Input Instructions

i.i.i input insi	ITUCUONS ARREST AND A TANK
EG 0.0	Interrogate interrupt number.
EG Y.O	Interrogate content of interrupt register.
EG Y.1	Interrogate keyboard code.
EG Y.2	Interrogate keyboard status bits.
Bit 1	LO, "reset" flag
	Bit 1 = "1": reset as result of an initial reset signal (output LOB on AG Y.2).
	This bit is reset by outputting MLO (bit 2) on AG Y.2.
Bit 2	PFS, parity error flag
	Bit 2 = "1": A parity error has occurred in the PSP during the information cycle of the last output instruction.
	This flag is reset by outputting MLO (bit 2) on AG Y.2.
Bit 3	LD, lost data
	Bit 3 = "1": Lost data, i.e. a new character has been entered from the key-board and the previous characte has not been picked up.
1. 14.	LD is reset by outputting MLO (bit 2) on AG Y

Bit 4 to 7 Not used

Bit 8 INT, interrupt flag

Bit 8 is set when a new character from the keyboard is made available. An interrupt is released if the interrupt condition is enabled. INT is reset by means of EG Y.1. Meltergabe sow a Vernierfaltgung disser Unterlage, servertrung und Mikelung hinse halbats nicht gestattet, sowell nicht ausstrückten tragsstanden für Archanstüngen serpflichten ubegändensstat, Kie Archanstüngen serpflichten ubegändensstat, Kie destind für der Archanstünung desti Gebrauchsmuster-Eintagung ünbekaten. We tergate sowie Verrieflätigung dieser Unterlage, verentung und Miktelium (Insele, "List inning gestattet, sowiet innih austrücklich upgestanden. La widerhandlungen verpflichten zu Schadenerstz. Alle Rechte für den Fall der Patenterleilung oder Gebräuchstrusster-färfragung vorbehalten.

• EG Y.3 Input individual characters

Bit 1 to 5 These 5 individual bits correspond to the 5 key-operated switches of the keyboard (They are not used on the 8870).

• EG Y.4 Interrogate display status bits

Bit 1 LO, delete flag

This flag is set when an initial reset has been performed by outputting LOB on AG Y.4. This flag is reset by outputting MLO (bit 2) on AG Y.4.

Bit 2 PFS, parity error flag

A parity error has occurred in the PSP during the information cycle of the last output instruction.

This flag is reset by outputting MLO (bit 2) on AG Y.4.

Bit 3 to 8 Not used

• EG Y.7 Input picture refresh memory
Interrogate picture refresh memory.

14.1.1.2 Output Instructions

• AG Y.1 Output indicator

Information for the keyboard lamps and the keyboard LED's is outputted.

information (Bit)	LED
1	1 (top LED)
2 907 1 1 2 3	2
3 42.10	3
4	4
5	5 (bottom LED)
6	yellow lamp
7 (5.65%) 42	red lamp adder (240 ms)
8	adder (240 ms)
	1 2 3 4 5 6 7

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AG Y.2 Output status Dividal hugal

Bit 1 modes LOB sale faubtvibni 2 seeds 2 of 1 sig

The DTEA is reset by outputting LOB. When this occurs LO is set in status line EG Y.2.

Bit 2 MLO MLO

The keyboard flag LO PFS on the status line EG Y.2 are reset by outputting MLO.

Bit 3 to 7 Not used

Bit 8 INT-KSP

Interrupt release by means of the keyboard is inhibited by outputting bit 8 = "l".

Bit 8 = "0": cancel interrupt inhibit

The flag INT (bit 8 on EG Y.2) is not affected when an interrupt is inhibites or reset.

• AG Y.4 Output operating status

The operating mode of the display is outputted.

Bit 1 LOB

The DTEA is reset when this bit is outputted. When this occurs bit 1 (LO) is set on line EG Y.4.

Bit 2 MLO

The flags LO and PFS on EG Y.4 are reset when MLO is outputted. $\label{eq:mlo}$

Bit 3 BS, Stall Moldamyolal auguno

Bit 3 = "1": The monitor is enabled for visual display.

visual display.

Ne regate sevia Vanta Hitgag disser Amerina yad Miteliurg Inter inters Amerina sevial net association usus Amerina amerina material amerina Processi amerina di Presentation

0 0 0 0 0

nteria nden nden satz.

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Bit 6	CI	
	Bit 6 = "1":	The monitor is enabled in the 960-character operating mode.
	Bit 6 = "0":	The monitor is enabled in the 480-character operating mode.

Bit 7	SU S A B I S A B B
	Bit 7 = "1": Page 1 is displayed with
	480 characters.
	Bit 7 = "0": Page 2 is displayed with 480 characters.

Bit 8 Not used

- AG Y.5 Output Y cursor

 Bits 1 to 4 These bits indicate the position of the cursor on the Y axis.
- AG Y.6 Output X cursor

 Bits 1 to 7 These bits indicate the position of the cursor
- AG Y.7 Output picture refresh memory
 This instruction loads the picture refresh memory.

on the X axis.

14.2 Interrupt Release

The DTEA can release interrupts. An interrupt can be released by depressing a key on the keyboard provided that the interrupt enable (bit 8 = "0") has been outputted on AG Y.2.

Interrupt release is not used with the 8870. The DTEA is controlled via the clock interrupt.

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14.3 Addressing

Addressing is via the coupling unit connected to the PSP interface.

Address structure

4	2	1	8	4	2	181
7	6	5	4	3 - 1 -	2	1
INF 6	INF 5	INF 4	INF3	INF 2	INF 1	INF 0
	7 INF 6	7 6 INF 6 INF 5	7 6 5 INF 6 INF 5 INF 4	7 6 5 4 INF 6 INF 5 INF 4 INF 3	7 6 5 4 3 INF6 INF5 INF4 INF3 INF2	7 6 5 4 3 2 INF6 INF5 INF4 INF3 INF2 INF1

Value
Bit
Information line

The addresses used at time of writing:

Address (with resp	ect to EG 0)	Work station	PSP bus
3.1.0	g elsoibat as	id along a of	1 1 1
3.1.8	. 2120	2.	1
3.2.0		3.	1
3.2.8	108100	4.	1
3.3.0		5.	1
3.3.8	n edepitori ed	14 46.49 1 01	1
3.4.0		W 947.00	1
3.4.8		8.	1
3.5.0	eester sinto	9.	V138
7.1.0		1.	2
7.1.8	two f notices:	2.	2
7.2.0		3.	2
7.2.8		4.	2
7.3.0		5.	2
7.3.8		6 seeslest room	2
7.4.0		7.	2
7.4.8	r na . szgovis	del glasiatina	2

There can only be 8 work stations on PSP bus 2 because the console must be on PSP bus 1.

Weitsfabb sow elverfeitätigung disser Unte
verweitung gund Missel missers infestis nich
statet sow elf regisseringklich spessioner
w Gernah ungen verti chren zu ehragenerstat
fische sich den han en Patternere ung des
transchungsfeitungsgegebeten.

Weitergabe sooi" verrieffaltigung gisser Unterlage, werenting und Weiterlaum in miss mitst nicht gestattet, soweit nicht ausdrücklich ungestanden. Lustattet, soweit nicht ausdrücklich ungestanden. Luschied zur den Fall der Patenterfellung oder Geziauchsmuster-Eintzagung vorbehalten.

14.4 Wiring Diagrams and Connector Assignment

33-pin SEL connector (BB)
PSP interface

Device connector assignment

1	GND
2	IFON
3	IF1N
4	IF2N
5	GND
6	IF3N
7	IF4N
8	IF5N
9	GND
10	IF6N
11	IF7N
12	PARN
13	GND
14	AGN
15	unused
16	STADN
17	GND
18	STIN
19	QUITTN
20	INTN
21	GND
22	INSAN
23	INSEN
24	NEN
25	LON
26	Uss
27	+ 5 V
28	+ 5 V
29	- 12 V
30	G ND
31	G ND
32	+ 24 V
33	+ 24 V

ocket	/	PZA	1	Contact	Signal
JOCKET		(6)	14.16	A	
			1200	B C	A3N
	•A		•C		A4N
		•B	12.1	163 E 8	GNE
	•D	•E	•F	D 8 E 8 F 9	A5N
	•H	●L	•K	H	A6N
	•11	•I	The state of the s	83 11 14	A7N
	•L		•N	K	
	-	•M	- M 1	83 L 81	
	•P		•S	M	
	1	•R		83 N	
	•T		•V	P	
		•U		R	GNI
	•W		•X	S	
			Vic		
Pin		PTA	P1 08	U	
1111		(0))	V	
	_	077	_/	W X	

Contacts are shown as seen on the pin wiring side.
20-pin Winchester connector SRE 20 PD NSS H 13

27 AUS7 N
28 WTAUS N
29 LOT N
30 NE N
31 ymsed
33 ymsed
34 ymsed
35 GND
35 GND
36 GND
37 GND



Contact arrangement of the 37-pin Cannon socket connector "D"

Og.

14

	sundo sorved
1	E1N0 N
2	E1N1 N
3	E1N2 N
4	E1N3 N
5	E1N4 N
6 7 8 9	EIN5 N EIN6 N EIN7 N KACT N unused
11 12 13 14 15	EBTO N EBT1 N EBT2 N EBT3 N EBT4 N
16	+ 5 V
17	+ 5 V
18	+ 5 V
19	+ 24 V
20	AUS0 N
21	AUS1 N
22	AUS2 N
23	AUS3 N
24	AUS4 N
25	AUS5 N
26	AUS6 N
27	AUS7 N
28	WTAUS N
29	LOT N
30	NE N
31	unused
32	unused
33	unused
34	GND
35	GND
36	GND
37	GND

V W +	

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