Field Engineering Manual

System 8870

Models 2, 4, and 6

Summary of I/O Card Assignments

4.79

1st Edition

Order Number: S 0445 101 04 79

NIXDORF
COMPUTER

Table of Contents

Index of abbreviations

AG	output
AWD	automatic dialling unit
BLZ	block length counter
DTEA	display-keyboard I/O unit
DÜST	communications control unit
EG	input
FB	busy flip-flop
GA	device address
KAR	head address register
KE	coupling unit
LKS	card punch
LMVG	read and compare
LSL	paper tape reader
LSS	paper tape punch
LVG	read and compare
PSP	parallel periphery interface
RAL	random access load
SPD	track difference counter
SS – N820	interface Nixdorf 820
WT	framing pulse
ZDV	line printer DMA feature

1 I/O 2802

The I/O is used as an interface converter from the SS 901 to the SS 820 and the PSP.

1.1 I/O Assignment

Instruct. \ Bit	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
EG 0.0.0.0											Interrupt number							
EG 0.0.X.0											interrupt number interrogation							
EG 0.0.X.1																PF	ZF	NA
EG 0.0.X.Y.Y.											dynamic input							
AG 0.0.X.0							0	0	0	0	interrupt number							
AG 0.0.X.0							1	0	0	0							INT PRI	INT SP
AG 0.0.X.1															reset FM	reset 820	reset PSP 2	reset PSP 1
AG 0.0.X.Y.Y											dynamic output							

X = Address of the coupling unit
Y = Address of peripheral equipment on the SSN 820 and the PSP

1.1.1 Description of I/O Assignment

There are 4 input and 3 output instructions.

1.1.1.1 Input Instructions

- EG 0.0.0 — Interrupt interrogation instruction
- EG X.0.0 — Interrogation instruction for the interrupt register of the coupling unit.
- EG X.0.1 — Interrogate status bits

  Bit 1 — The SS-N820 has signalled a power failure.

  Bit 2 — Time fault in the PSP.

  A time fault is present if there is no acknowledge signal within 2.4 us after "start information" is outputted.

  Bits 1 and 2 can be outputted in combination.

  Bit 3 — Parity error in the PSP.
- EG X.Y.Y — Input instruction for peripheral equipment.

1.1.1.2 Output Instructions

- AG X.0.0 — Output the interrupt number, the interrupt disable or interrupt enable and the interrupt priority definition.

  Bit 12 — Bit 12 = "0"
  Interrupt number is outputted in bits 1 to 8.

  Bit 12 = "1" and bit 1 = "0"
  The interrupt disable is cancelled.

  Bit 12 = "1" and bit 1 = "1"
  The interrupt number disable is implemented.

  Bit 12 = "1" and bit 2 = "0"
  the interrupt of the SS-N820 has highest priority.

  Bit 12 = "1" and bit 2 = "1"
  The interrupt of the disk store has highest priority.

- AG X.0.1 Delete status bits

  Bit 1 Is used to generate the clear signal on PSP bus 1.

  Bit 1 is to be outputted twice, once as "1" (delete is outputted), and once as "0" (delete is cancelled).

  Bit 2 Is used to generate the clear signal on PSP bus 2.

  Bit 2 is to be outputted twice, once as "1" (delete is outputted), and once as "0" (delete is cancelled).

  Bit 3 Is used to generate the clear signal on SS-N820.

  Bit 3 is to be outputted twice, once as "1" (delete is outputted), and once as "0" (delete is cancelled).

  Bit 4 Is used to delete error flags ZF (time error) and PF (parity error).

- AG X.Y.Y Output instruction to operate peripheral device.

1.2 Coupling Unit (KE) 2802 Interrupt Release

The KE does not itself generate interrupt signals i.e. interrupt triggering is by recognition of an interrupt signal from a peripheral device. The interrupt number which is thus generated consists of both the interrupt number of the KE and the interrupt number of the peripheral device.

1.3 KE 2802 Addressing

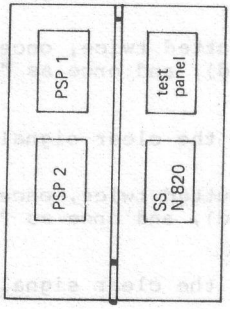
Address 4.0.0 = Internal I/O instruction and I/O instruction for the SS-N820

Address 5.0.0 = I/O instruction for SS-N820

Address 3.0.0 = I/O instruction for PSP bus 1

Address 7.0.0 = I/O instruction for PSP bus 2

1.4 Physical Layout



1.5 Test Point Assignment of the 820 Test Panel

Top view of contact side

E1N ●	A1N ●	D1N ●
E2N ●	A2N ●	D2N ●
E3N ●	A3N ●	D3N ●
E4N ●	A4N ●	D4N ●
E5N ●	A5N ●	D5N ●
E6N ●	A6N ●	D6N ●
E7N ●	A7N ●	D7N ●
E8N ●	A8N ●	D8N ●
E9N ●	A9N ●	D9N ●
E10N ●	A10N ●	D10N ●
E11N ●	A11N ●	D11N ●
E12N ●	A12N ●	EANFN ●
NAN ●	INSEN ●	EAIRN ●
EGN ●	AGN ●	LO ●

2 Printer Connection to PSP via KE 2802

2.1 I/O Assignment of the 4552.xx Printer to the PSP

Row \ Bit	8	7	6	5	4	3	2	1
EG 0.0	← interrupt number →							
EG Y.0	← interrupt number (always) →							
EG Y.1		DF print error	PF paper error	VR feed active	DR printer active	PAE end of paper	DATANF request for data	KLAR (ready)
EG Y.2	INT	INT test		INT end of feed	INT end of print	INT end of block	PSP parity error	delete
EG Y.3	← type of printer →		← type of drum →					
AG 0.1	← data for block transmission →							
AG Y.0	← interrupt number →							
AG Y.1	← data for direct transfer →							
AG Y.2	← control character →							
AG Y.3	← start print position →							
AG Y.4	← feed information → (line)							

2.1.1 Description of I/O Assignment

There are 5 input and 5 output instructions.

2.1.1.1 Input Instructions

- EG 0.0.0 Interrogate Interrupt number
- EG X.Y.0 Interrogate the interrupt register of the printer control unit
- EG Y.1 Printer status bits

Bit 1 KLAR (ready)

This bit is set if the printer is ready to operate.

Note that this bit is only set if:

a) The printer is switched on,

b) The drum arm is closed,

c) The printer drum has reached its normal running speed,

d) the punched tape of the channel feed device has been read in, if the latter is switched on,

e) No print hammer fault,

f) No ink ribbon fault,

g) No format fault,

h) No paper fault,

i) No incorrect character has been transferred,

k) The previous paper feed was completed within 2.5 s,

l) There is no fault in the punched tape and

m) A non-punched channel of the feed tape has not been selected.

Bit 2 DATANF

This bit is set when the printer is ready to accept data.

Bit 3 PAE

This bit is set when end of paper is reached.

Bit 4 DR

This bit is set when a printing process is being carried out.

Bit 5 VR

This bit is set when paper is being fed.

Bit 6 PF

This bit is set when the following conditions are satisfied:

a) A feed fault has occurred,

b) The paper has run out of the tractor,

c) Paper feed has not been completed within 2.5 s,

d) PAE (end of paper) is set and the last line of the form has reached the printing station.

Bit 7 DF

This bit is set if there is a print error.

The following conditions entail the setting of bit 7:

An incorrect character has been presented for processing or there is a print hammer fault.

Bit 8 Not applicable

• EG X.Y.2 Interrogate cause of interrupt

Bit 1 Delete

this bit is set if the printer was switched off, or if there was a power failure.

Bit 2 Parity error

this bit is set if a parity error is detected during data transmission in the PSP.

Bit 3 End of block interrupt

this bit is set if the end of block character is detected in the printer during automatic data transmission (only in the DMA operational mode).

Bit 4 End of print interrupt

This bit is set at the end of a printing process .

Bit 5 Feed interrupt

This bit is set when feed has been completed.

Bit 6 Not applicable

Bit 7 Check interrupt

This bit is set when a check interrupt is released.

Bit 8 Interrupt

This bit provides a general indication that an interrupt is present and appears together with every interrupt.

- EG X.Y.3 Interrogate drum and printer type

Drum type: Various types of drums with different character sequences and founts can be used in conjunction with the printer equipment. The table below gives details of available drum types and their respective codes. Coding is by means of inserting the relevant PROM card assigned to each drum type.

Bit assignment	5	4	3	2	1	Designation of drum type
	0	0	0	0	0	ASCII-DP 64-character
	0	0	0	0	1	ASCII-DP 96-character
	0	0	0	1	0	Standard 64-character 60-character set: OCR-B1
	0	0	0	1	1	Standard 96-character 96-character set: ORC-B1

Printer type: Bits 7 and 8 indicate the type of printer.

Bit assignment	7	6	Line printer
	1	0	Print speed 300 lines/minute
	1	1	Print speed 600 lines/minute

2.1.1.2 Output Instructions

- AG 0.1 — This is not an output instruction. The AG 0.1 statement relates to automatic data transmission; automatic data transmission is initialized by AG 0.1.

- AG X.Y.0 — The interrupt number is outputted to the interrupt register of the printer.

- AG X.Y.1 — Print data is outputted by the CPU (central processing unit) to the printer direct (no DMA mode).

- AG X.Y.2 — Control characters transferred to the printer.

Instruction code	Meaning
0.0	Release interrupt disable
0.1	Delete all flags (general deletion) and implement interrupt disable
0.2	Delete "PSP parity error" and "delete" flags
0.3	Start DMA (set ANFR for automatic data transmission)
0.4	Delete "Int. end of block" flag
0.5	Delete "Int. end of print" flag
0.6	Delete "Int. end of feed" flag
0.7	
0.8	Delete "Check interrupt" flag
0.9	Release check interrupt
0.10	
0.11	
0.12	
0.13	release printing
8.0	disable interrupt

- AG X.Y.3 — Output start print position.

- AG X.Y.4 Feed information output

  Bit 1 to 7 These bits contain the value for the feed dependng on the content of bit 5.

  If bit 5 = "1" then bits 1 to 4 and bits 6 and 7 contain the number of line feeds.

  If bit 5 = "0" then bits 1 to 4 contain the channel number of the channel feed.

2.2 Interrupt Release

The completion of a printing process is signalled by an interrupt. Any fault conditions are likewise signalled to the system by an interrupt.

2.3 Addressing

Address bits 5 to 8 are used for addressing.

Address X.Y.Z

X = KE 2802 of DSZ 1804 address
Y = Printer control address
Z = Line

3 I/O 0317.03

The I/O is used to drive the 0611 magnetic tape on the 8870 system (recording density 800 bits per inch).

3.1 I/O Assignment

Row \ Bit	12	11	10	9	8	7	6	5	4	3	2	1
EG Y.1				channel 9	channel 8	channel 7	channel 6	read channel 5	channel 4	channel 3	channel 2	channel 1
EG Y.2				Write Enable	Rewinding	Ready	Beginning of Tape	parity and echo error	temp. error	End of Tape	Bit detected	Write Power
EG Y.4										buffer empty (read)	buffer full (write)	end of block detector
EG Y.8												
EG Y + 2.0	CRC arithmetic unit			channel 9	channel 8	channel 7	channel 6	channel 5	channel 4	channel 3	channel 2	channel 1
AG Y.1				channel 9	channel 8	channel 7	channel 6	write channel 5	channel 4	channel 3	channel 2	channel 1
AG Y.2								Rewind + Lockout	Rewind	Write Permit	Forw.(1) Rev. (0)	Run (1) Stop (0)
AG Y.4	clear input store											
AG Y.8												
AG Y + 2.0							Parity ODD (1) EVEN (0)	clear CRC register	read enable			

3.1.1 Description of I/O Assignment

The following I/O instructions are available in the operating program for the control of the magnetic tape station via the I/O 0317.03.

3.1.1.1 Input Instructions

- EG Y.1

  Bit 1 - 9 Read in character from tape.

- EG Y.2 Status messages

  Bit 1 Write power, i.e. erase and write heads are switched on.

  Bit 2 Bit detected

  Not evaluated by channel program.

  Bit 3 End of tape (EOT)

  End of tape mark detected. This message is stored in a flip-flop.

  Bit 4 Temperature error

  Temperature sensor indicates that permissible tape deck temperature has been exceeded.

  Bit 5 Parity or echo error

  Not evaluated by channel program.

  Bit 6 Beginning of tape (BOT)

  Beginning of tape mark detected at photodiode.

  Bit 7 Ready

  The tape deck is switched to "remote" and ready to operate.

  Bit 8 Rewinding

  The tape deck is rewinding and has not yet reached BOT.

  Bit 9 Write enable

  Write is enabled because write enable ring is loaded (write enable contact closed).

- EG Y.4

  Bit 1 — Block end message

  Not evaluated by channel program.

  Bit 2 — Buffer full (write)

  Message from FIFO, i.e. buffer contains 64 characters.

  Bit 3 — Buffer empty (read)

  The message resets, a write flip-flop and switches over to "read".

- EG Y + 2.0 — CRC arithmetic unit

  The CRC character formed in the arithmetic unit register is ready.

3.1.1.2 Output Instructions

- AG Y.1

  Bits 1 - 9 — Write Information

- AG Y.2 — Control bits

  Run/stop — 1 = Run, 0 = Stop

  Bit 2 — Forward/reverse — 1 = Forward, 0 = Reverse

  Bit 3 — Write permit

  (write permit)

  Bit 4 — Rewind

  The tape is wound back to the beginning of tape mark (BOT).

  Bit 5 — Rewind and lock out

  In addition to rewind, the tape is wound past BOT, the tape station switches to "reset" and the vacuum is switched off.

- AG Y.4 — Clear input store

  All status flip-flops and the system are reset.

- AG Y + 2.0

  Bit 4 Read enable
  Specific release of buffer for "read" or "check read".

  Bit 5 Clear CRC register
  i.e. null exchange

  Bit 6 Parity 1 = ODD parity
  0 = EVEN parity

3.2 Interrupt Release

The I/O 0317.03 cannot be interrupted and is controlled via the clock interrupt.

3.3 Addressing

Address bits 5 to 8 are used. Bit 6 has a special function and is used to address the CRC arithmetic unit, the read enable etc.

The addresses used at time of writing are as follows:

X.1.4 = 1. I/O - 0317.03
X.4.0 = 2. I/O - 0317.03

X = KE address = 4.0.0

4 I/O 0318

The I/O is used to control the magnetic tape cassette.

4.1 I/O Assignment

Row \ Bit	12	11	10	9	8	7	6	5	4	3	2	1
EG 0.0												
EG Y.1	code error	read bit number error	read parity error	RAL reader	buffer status	read CRC error	time error	write parity error	end of operation	write inhibit	end of tape	ready
EG Y.2				Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
EG Y.3	input data								Bit 8	Bit 7	Bit 6	Bit 5
EG Y.4									input data			
EG Y.5										eject container full	change process is running	hopper empty
AG 0.0									I/O card address			0=cassette 0 1=cassette 1
AG Y.1				control code of deck								
AG Y.2				Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
AG Y.3	output data								Bit 8	Bit 7	Bit 6	Bit 5
AG Y.4									output data			
AG Y.5	control code change mechanism											

4.1.1 Description of I/O Assignment

3 input and 4 output instructions are required to control the cassette.

4.1.1.1 Input Instructions

- EG X.Y.1 Interrogate status bits

  Bit 1 Ready

  The cassette is ready to operate.

  Bit 2 End of tape

  The end of tape has been detected in the cassette.

  Bit 3 Write inhibit

  There is a write inhibit for the actual cassette in the deck.

  Bit 4 End of operation

  A write or read operation has been completed.

  Bit 5 Write parity error

  A parity error has been detected during a write operation.

  Bit 6 Time error

  There is a write time error if the 4-character buffer and the shift register become empty during a write operation.

  There is a read time error if the 4-character buffer and the shift register become full during a read operation.

  Bit 7 CRC error

  The computed check character differs from the read in check character (check character = CRC character).

Bit 8 Buffer status

This bit provides information concerning the status of the 4-character buffer.

"Read" operation: The bit is set when the first character is transmitted to the 4-character buffer. If remains set as long as the buffer contains characters.

"Write" operation: The bit is set when there are 4 characters in the 4-character buffer (buffer full).

Bit 9 RAL reader

If bit 9 is set a cassette RAL reader is connected.

Bit 10 Parity error

A parity error has occurred during a read operation.

Bit 11 Bit number error during read

During the read operation a data character other than the 9-bit character has been detected.

Bit 12 Code error

The outputted control code is not valid for the cassette transport.

• EG X.Y.2 Interrogate input data for 8-bit character processing.

Bits 1 - 9 These bits contain the code of the input character.

Bit 10 Not applicable

Bit 11 Track location

This bit denotes whether the A or B side of the cassette is being used. Not used for the 900 M1 and the 8870.

Bit 12 Bit 12 denotes whether an operation was completed without any fault.

Bit 12 = "1" = Operation satisfactory
Bit 12 = "0" = Operation unsatisfactory

This bit is not used for the 900 M1 and the 8870.

- EG X.Y.3 Interrogate input for 4-bit charcter processing (system 820 only).

  This input instruction is not used for the 8870 (8-bit processing only).

- EG X.Y.5 Status bits for cassette RAL reader.

  Bit 1 Hopper empty

  Bit 2 Change process is running

  Bit 3 Eject container full

4.1.1.2 Output Instructions

- AG X.Y.0 Preselection of I/O 0318 and connected cassette.

  Bit 1 Bit 1 selects one of the two cassettes connected to the I/O for the next I/O operation.

  Bit 1 = "0" = the first cassette of the I/O is selected.

  Bit 1 = "1" = the second cassette of the I/O is selected.

  Bits 2 - 4 These bits contain the preselection address for the I/O 0318 to be addressed.

- AG X.Y.1 Output control code for cassette drive.

  Table of control codes

Control code	Instruction
0.0	Stop operation
0.3	Write check character
0.5	4-bit data format changeover
0.6	8-bit data format changeover
0.9	Clear status detector
3.0	Open cover
3.3	Reset one block without erase
3.5	Run forward to BOT without erase
3.6	Rewind to leader tape
3.8	Pay off
3.9	Read block
6.3	Reset one block with erase
6.5	Run forward to BOT with erase
6.8	Write block with long block gap
6.9	Write block with normal block gap

- AG X.Y.2 — Output data characters for write operation.

  This instruction loads the output character into the 4-character buffer of the I/O.

- AG X.Y.3 — This instruction is used only for 4-bit character processing (820 system).

- AG X.Y.5 — Control code for change mechanism.

  Output control code for change mechanism of cassette RAL reader.

Control code	Instruction
3.0	Retract head, cover open
3.3	Unlock and rewind

4.2 Interrupt Release

The I/O 0318 cannot be interrupted and is controlled by the clock interrupt.

4.3 Addressing

The preselection address and the I/O address are used.

The instruction AG X.Y.0 is used for the preselection address, the selection address being in bits 1 to 4.

The I/O address used at the time of writing is X.C.0.
X = KE 2802 address (= 4.0.0)

I/O	Address	Pre-Selection
1. I/O	12.12.0	0.0 or 0.1
2. I/O	12.12.0	0.2 or 0.3

For notes

5 I/O 0325

5.1 I/O Assignment for Printer 4550.03 with Genuine DP Electronics and 0817.01

Bit	12	11	10	9	8	7	6	5	4	3	2	1	
EG X.Y.1	Fault	0			Safety switch	Light detect		feed	Busy	Select		end of paper	*1
EG X.Y.1	0	1			1	1		1	Data Demand	0		0	
EG X.Y.2	Fault	0			Safety switch	Light detect		Vorschub	Busy	Select		end of paper	*2
EG X.Y.2	0	1			1	1		1	Data Demand	0		0	
AG X.Y.1		Paper Instr. "PI"		Strobe	Data 8	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	*3
AG X.Y.2		Paper Instr. "PI"		Strobe	Data 8	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	

*1 1. printer 0817.01 or 1. printer 4550.03

*2 2. printer 0817.01 or 2. printer 4550.03

*3 1. printer 0817.01 or 2. printer 0817.01 or 4550.03

5.1.1 Description of I/O Assignment

(When cable 7032.03 is used for connection of printer 4550.03 and 0817.01).

There are 2 input and 2 output instructions.

5.1.1.1 Input Instructions

- EG X.Y.1 Interrogate printer 455.03 status bits.

  Bits 1 - 3 Not used

  Bit 4 Data demand, equivalent to "request" signal.

  Bit 5 Always "1"

  Bit 6 Not used

  Bits 7 and 8 Always "1"

  Bits 9 and 10 Not used

  Bit 11 Always "1" (Recognition bit for printer 0817.01)

  Bit 12 Not used

- EG X.Y.2 Interrogate printer 0817.01 status bits

  Bit 1 End of paper

  Bit 2 Not used

  Bit 3 Printer select bit, switch printer to on-line

  Bit 4 Busy, printer ready to operate

  Bit 5 Paper feed is running

  Bit 6 Not used

  Bit 7 Light defect (positioning error), only when the positioning lamp is defective.

Bit 8 — Safety switch indicator on right hand side of carrier (no longer fitted for some time, therefore always "1").

Bits 9 and 10 — Not used

Bit 11 — Distinction bit for printer 0817.01 (Bit 11 = "0") and printer 4550.03 (Bit 11 = "1")

Bit 12 — Fault

Printer hardware fault

5.1.1.2 Output Instructions

- AG X.Y.1 — Output printer characters, control characters and feed information for printer 4550.03.

Bit 1 - 8 — Output information bits

A data character or a control character may be outputted.

Control character

Symbol	Code	Meaning
CR	0.13	Print release
LF	0.10	Line switch
FF	0.12	Line switch by channel feed

Bit 9 — Strobe bit

Each information item in bits 1 to 8 is outputted once with the strobe bit and once without the strobe bit.
Strobe = Information transfer signal.

Bit 10 — Not used

Bit 11 — Paper instruction bit

If bit 11 is set there is line feed information in bits 1 to 8. Bit 5 is used to differentiate between line feed and channel feed. Line feed information in bits 1 to 4 and in bits 6 and 7.

Bit 5 = "0": Implement line feed (63 lines max.)

Bit 5 = "1": Implement channel feed (channel number in bits 1 to 4)

Bit 12 Not used

- AG X.Y.2 Output print character, control character and line feed for printer 0817.01.

  See AG X.Y.1 for bit assignment.

5.2 Interrupt Release

The I/O 0325 cannot be interrupted and printer control is via the clock interrupt.

5.3 Addressing

Bits 5 to 8 of the address to be outputted are used. At the time of writing address X.D.1 is used.
X = KE 2802 address

5.4 I/O Assignment for Data Product Printer 4552 with Nixdorf Electronic Equipment

Row \ Bit	12	11	10	9	8	7	6	5	4	3	2	1
EG X.Y.1										PAEN	DANFN	READY
AG X.Y.1				DASTRN	IF 7 N	IF 6	IF 5	IF 4	IF 3	IF 2	IF 1	IF 0

5.4.1 Description of I/O Assignment using Connection Cable 7032.02

There is one input and one output instruction.

5.4.1.1 Input Instructions

- EG X.Y.1 Interrogate printer status bits.

Bit 1 READY

The printer is ready to operate.

Bit 2 DANFN (Data request)

Data request is the acknowledge signal for the transfer of characters and instructions to the printer. It is "1" (DANFN = 0V) if the printer is waiting for data. After each transfer of a character (DASTR) DANF becomes "0" for at least 250 ns.
DANF = "0" while the printer is printing.
DANF = "1" when the printer paper feed is operating and data can be transferred

In principle data can only be transferred to the printer if DANF has previously been interrogated as "1".

Bit 3 PAEN

End of paper (lower switch).

5.4.1.2 Output Instructions

- AG X.Y.1 Output information

Bits 1 - 7 These are information bits and contain the character and instruction codes for the printer.

Instruction character codes

Symbol	Code	Meaning
CR	0.13	Print release
LF	0.10	Line feed
FF	0.12	Line feed by channel feed

Bit 8 — If bit 8 is set then there is line feed information in bits 1 to 7. The content of bit 5 determines whether line or channel feed is carried out.

Bit 5 = "1": Line switch (63 max).

Bit 5 = "0": Channel feed (channel number in bits 1 to 4)

Bit 9 — Strobe bit, information transfer bit.

Each information item is outputted once with the strobe bit and once without the strobe bit.

Bits 10 to 12 — Not used

5.5 Interrupt Release

The I/O 0325 cannot be interrupted. Printer control is via the clock interrupt.

5.6 Addressing

Bits 5 to 8 of the outputted address are used. At the time of writing the address X.D.1 is used (X = KE 2802 address).

For notes

6 I/O 0327

The I/O 0327 is used to control the daisy-chain line.

6.1 I/O Assignment

Row \ Bit	a 12	a 11	a 10	a 9	a 8	a 7	a 6	a 5	a 4	a 3	a 2	a 1
EG Y.1	e 12 status bit S 12	e 11 status bit S 11	e 10 status bit S 10	e 9 parity bit	e 8 data bit	e 7	e 6	e 5	e 4	e 3	e 2	e 1 data bit
EG Y.2	M12=„1" send buffer busy								M4 ANB≙ rdy. call	M3 transfer taking place	M2 parity error	
AG Y.1					data bit							
AG Y.2											Reset M 2	1 = comm. 0 = Term.
AG Y.4					for OP code with local data transm.	0 = Select 1 = Poll	IDN address bits					

6.1.1 Description of I/O Assignment

There are two input and three output instructions.

6.1.1.1 Input Instructions

- EG X.Y.1 Interrogate status bits and input data.

  Bits 1 to 8 Received character

  Bit 9 The parity bit allocated to the received character.

  Bits 10 to 12 Status bits S 10 to S 12

  Meaning of status bits

S 12	S 11	S 10	In the communications control unit (DUST)	In terminal
0	0	0	No POLL / SELECT procedure or garbled character on line	No character received
0	0	1	Polled / Selected → Terminal not → ready to transmit / ready to receive or a terminal parity error is detected	Does not happen
0	1	1	Polled / Selected → Terminal not ready to operate	Does not happen
0	1	1	Data character / Acknowledge character → contained parity error	A character with incorrect parity was received
1	0	0	The communications control unit (DUST) received a correct character The terminal received a character correctly	A correct character was received

- EG X.Y.2 Interrogate flag bits

  Bit 2 Flag bit 2

  A parity error has ocurred during data transfer.

  Bit 3 Flag bit 3

  A data transfer process is taking place.

  Bit 4 Flag bit 4

  the I/O is ready for receiving. Applies in the "DUST" and "Terminal" operating modes. Bit 4 is reset when an address character is detected on the line (no longer ready for receiving).

  Bit 12 Flag bit 12

  The send buffer is busy.

6.1.1.2 Output Instructions

- AG X.Y.1 Load data characters into send buffer.

  Bits 1 to 8 Data characters to be outputted.

- AG X.Y.2 Output operating mode

  Bit 1 Bit 1 = "0": The I/O is switched to the "Terminal" operating mode, i.e. is passive.

  Bit 1 = "1": The I/O is switched to the "DUST" operating mode, i.e. is active.

  Bit 2 Reset M2

  The "parity error" flag is reset.

- AG X.Y.4 Output address character

Bits 1 to 6 Address character to be outputted.

Bit 7 This bit determines whether a data character is to be transmitted or a data character is to be received after the address which has been transmitted.

Bit 7 = "0": A data character is received after the address character has been transmitted (select).

Bit 7 = "1": A data character is transmitted after the address character has been transmitted (poll).

Bit 8 This bit determines whether characters are transmitted singly or in sets.

Bit 8 = "0": Transmission of single characters
Bit 8 = "1": Transmission of character sets

Only possible with local data transmission.

6.2 Interrupt Release

The I/O 0327 cannot be interrupted and is controlled by the clock interrupt or by an external I/O interrupt, e.g. I/O - 1806 interrupt.

6.3 Addressing

Bits 5 to 9 of the address to be outputted are used to address the I/O. At the time of writing the address 1.9.0 is used for the first I/O and the address 1.A.0 is used for the second I/O. (Remember the KE 2802 address).

7 I/O 1801

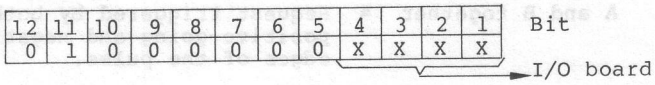
The I/O 1801 is used to control low-speed peripheral devices such as the card reader, the card punch, the tape reader and the tape punch. The assignment of the I/O therefore depends on the connecting cable used (see various connecting cable types).

7.1 I/O 1801 Addressing

The I/O 1801 is addressed by means of preselection and the board address.

Preselection is via the instruction AG 0 with bit 11 set and the board number in bits 1 to 4.

- Board preselection



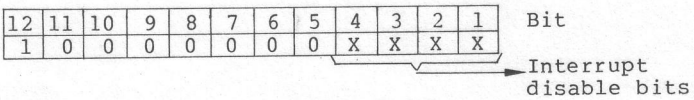
The I/O address used at the time of writing is 4.A.X.

4.0.0 = KE address
0.A.0 = I/O 1801 address
X = Line address

7.2 Interrupt Release

The I/O 1801 does not generate any internal interrupt and can only evaluate interrupts from peripheral equipment (set internal interrupt flags) and inform the central processing unit (interrupt channel). A total of 4 interrupts can be stored.

Interrupt flags (interrupt channels) can be disabled or enabled by means of instruction AG 0 with bit 12 set.



Interrupt disable bit = "1": Implement interrupt disable.

Interrupt disable bit = "0": Cancel interrupt disable.

- Interrupt assignment for the 120-pin Ericsson connector of the I/O 1801.

Signal path	A99	A94	A89	A84	A79	A74	A69	A64
Interrupts	4B	4A	3B	3A	2B	2A	1B	1A
	4. Interrupt		3. Interrupt		2. Interrupt		1. Interrupt	

The letters A and B indicate whether the interrupt request from the peripheral eqipment is triggered by the negative-going or the positive-going edge of the pulse.

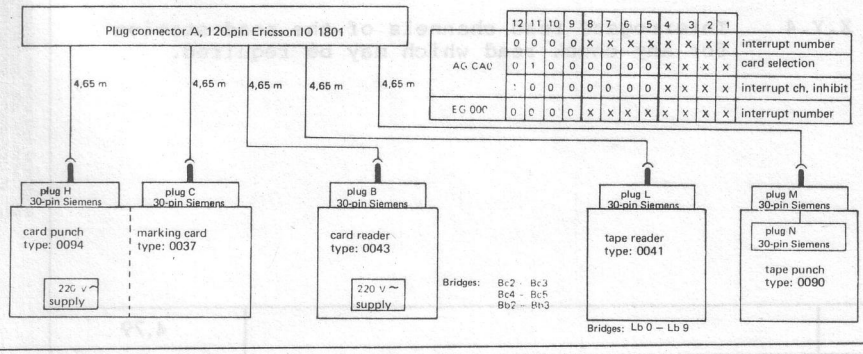
A = Request triggered by the negative-going edge of the pulse.

B = Request triggered by the positive-going edge of the pulse.

A and B together = Request triggered by both the positive-going and negative-going edges of the pulse.

The request for the interrupt bit is a result of the input instruction EG 0.

	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
EG 4.A.1	tape reader no inter.	tape reader tape change	tape reader framing pulse 2	tape reader framing pulse 1	tape reader channel 8	tape reader channel 7	tape reader channel 6	tape reader channel 5	tape reader channel 4	tape reader channel 3	tape reader channel 2	tape reader channel 1
Signal path	A 56 Lb 1	A 51 Lc 0	A 46 LA 0	A 41 La 9	A 36 La 8	A 31 La 7	A 26 La 6	A 21 La 5	A 16 La 4	A 11 La 3	A 6 La 2	A 1 La 1
EG 4.A.2	card reader no inter.	card reader multi-punching ch.11-7	card reader framing pulse 2	card reader framing pulse 1	card reader channel 8	card reader channel 9	card reader channel 12	card reader channel 11	card reader channel 0	card reader	card reader channel 1-7	card reader
Signal path	A 57 Ba 0	A 52 Bb 2	A 47 Ba 2	A 42 Ba 1	A 37 Bb 1	A 32 Ba 6	A 27 Ba 9	A 22 Ba 8	A 17 Ba 7	A 12 Ba 5	A 7 Ba 4	A 2 Ba 3
EG 4.A.3	tape punch end of paper punch error	TZL Ready	tape punch pilot hole	tape punch timing			card punch change punch magnet	card punch card in read station	card punch card in punch station	card punch submit inhibit	card punch switch off card feed	card punch punch inhibit
Signal path	A 58 Mc 3, Nc 3	A 53 Bb 8	A 48 Ma 0	A 43 Ma 1	A 38	A 33	A 28 Hc 4	A 23 Cb 3	A 18 Hc 7	A 13 Hc 6	A 8 Hc 5	A 3 Hc 1, Hc 8, 9
EG 4.A.4	card punch channel 12	card punch channel 11	card punch channel 0	card punch channel 1	card punch channel 2	card punch channel 3	card punch channel 4	card punch channel 5	card punch channel 6	card punch channel 7	card punch channel 8	card punch channel 9
Signal path	A 59 Cb 2	A 54 Cb 1	A 49 Ca 0	A 44 Ca 1	A 39 Ca 2	A 34 Ca 3	A 29 Ca 4	A 24 Ca 5	A 19 Ca 6	A 14 Ca 7	A 9 Ca 8	A 4 Ca 9
EG 4.A.5												
Signal path	A 60	A 55	A 50	A 45	A 40	A 35	A 30	A 25	A 20	A 15	A 10	A 5
AG C.A.1				tape punch release	tape punch punch magnet 8	tape punch punch magnet 7	tape punch punch magnet 6	tape punch punch magnet 5	tape punch punch magnet 4	tape punch punch magnet 3	tape punch punch magnet 2	tape punch punch magnet 1
Signal path	A 116	A 111	A 106	A 101 Mb 9	A 96 Mb 8	A 91 Mb 7	A 86 Mb 6	A 81 Mb 5	A 76 Mb 4	A 71 Mb3	A 66 Mb 2	A 61 Mb1
AG C.A.2	LSL Start	LSL Stop		card reader feed magnets					card punch step off	card punch step on	card punch card feed	card punch motor
Signal path	A 117 Lc 1	A 112 Lc2	A 107	A 102 Bc 6	A 97	A 92	A 87	A 82	A 77 Hb 7	A 72 Hb 8	A 67 Hb 4	A 62 Hb 3
AG C.A.3	card punch punch magnet 12	card punch punch magnet 11	card punch punch magnet 10	card punch punch magnet 9	card punch punch magnet 8	card punch punch magnet 7	card punch punch magnet 6	card punch punch magnet 5	card punch punch magnet 4	card punch punch magnet 3	card punch punch magnet 2	card punch punch magnet 1
Signal path	A 118 Hb 2	A 113 Hb 1	A 108 Ha 0	A 103 Ha 1	A 98 Ha 2	A 93 Ha 3	A 88 Ha 4	A 83 Ha 5	A 78 Ha 6	A 73 Ha 7	A 68 Ha 8	A 63 Ha 9
Interrupt					4 B	4 A	3 B	3 A	2 B	2 A	1 B	1 A
Signal path	A 119	A 114	A 109	A 104	A 99	A 94	A 89 Ma 1	A 84 Ma 1	A 79	A 74 Lc 4	A 68	A 64 Bb 5
Power supply	0 V	0 V	0 V	0 V	+ 36 V	+ 36 V	+ 24 V	+ 6 V		30 V		
	A 120	A 115	A 110	A 105	A 100	A 95	A 90	A 85	A 80	A 75	A 70	A 65
	Hb 0 3x Cb 0 3x Bb 0 2x Bb 4 2x				Hb 5 2x Bc 4 2x Bc 5 2x		Hb 9 2x Bb 9 2x	Cb 6 2x				



7.3 I/O Assignment using Connecting Cable 7034

7.3.1 Description of I/O Assignment for Card Punch 0095.00 or 0095.01

The punch is connected to the I/O 1801 via cable 7034.

Two input instructions and two output instructions are required to operate the punch.

7.3.1.1 Input Instructions

- EG X.Y.3 — Interrogate punch status bits

  Bit 1 — Punch inhibit

  This instruction is inputted when the hopper is empty, when the stacker is full, when a card is being fed and when the manual card release control is actuated and the motor is running up (after switching on).

  Bit 2 — Switch off card feed

  Cancel card feed magnet (switch off coupling magnet).

  Bit 3 — Submit inhibit

  This bit is set up to the end of the card feed operation.

  Bit 4 — Card in punch station

  This bit is set when there is a card in the punch station.

  Bit 5 — Card in read station

  Message from read channel 13 (card in read station).

  Bit 6 — Change punch magnet

  This bit is set before the next column punch to be carried out.

- EG X.Y.4 — Interrogate read channels of the read station for any check read which may be required.

7.3.1.2 Output Instructions

- AG X.Y.2 Output operating mode bits

  Bit 1 Motor on

  This bit is outputted to start the card punch motor. (There is a delay whilst the motor runs up and punch inhibit is implemented during this period).

  Bit 2 Card feed

  This bit addresses the coupling magnet and releases a card feed.

  Bit 3 Step on

  This bit switches on the step-by-step transport of a card through the punch station.

  Bit 4 Step off

  This bit switches off the step-by-step transport of a card through the punch station (after the last column has been punched).

- AG X.Y.3 Output punch information

7.3.2 Interrupt Release

The punch does not release any interrupts and is controlled by the clock interrupt.

7.3.3 Addressing

See Section 7.1.

7.4 I/O Assignment for Card Reader 0043.03

7.4.1 Description of I/O Assignment

The reader is connected to the I/O 1801 via cable 7034. One input instruction and one output instruction are required to operate the reader.

7.4.1.1 Input Instructions

- EG X.Y.2 Interrogation instruction for acceptance of information and status bits.

  Bits 1 to 3 These bits show the coded information from card reader channels 1 to 7.

  Bit 4 Information from card reader channel 0.

  Bit 5 Information from card reader channel 11.

  Bit 6 Information from card reader channel 12.

  Bit 7 Information from card reader channel 9.

  Bit 8 Information from card reader channel 8.

  Bits 9 and 10 Indicator for the card reader framing bits.

  Sequence of framing bits:
  0, 1, 2, 3, 0, 1, 2, 3 etc.

  Bit 11 Multi-punch in channels 1 to 7, i.e. more than one hole is punched in columns 1 to 7.

  Bit 12 "No interrogation" message

  When this message is present the interrogation of read channels is not permitted.

7.4.1.2 Output Instructions

- AG X.Y.2 Output "start reader"

  Bit 9 Bit 9 is used to "start" or "stop" the reader.

  Bit 9 = "1": start reader
  Bit 9 = "0": stop reader

7.4.2 Interrupt Release

An interrupt is released to inform the system each time a card column is read.

7.4.3 Addressing

See Section 7.1.

7.5 I/O Assignment for Card Reader 0041.01

7.5.1 Description of I/O Assignment

The reader is connected to the I/O 1801 via cable 7034.

One input instruction and one output instruction are required to operate the reader.

7.5.1.1 Input Instructions

- EG X.Y.1 — Interrogate character information and status bits.

  Bit 1 to 8 — Read channel information from channels 1 to 8.

  Bits 9 and 10 — Framing pulses 1 and 2

  Control signals for the recognition of individual rows of the punched tape. The status of these signals changes from row to row in the following sequence: 2, 0, 1, 3.

  Bit 11 — Tape change

  This bit is set when a tape is in the read station.

  Bit 12 — No interrogation

  When "no interrogation" is set the information contained in bits 1 to 8 must not be evaluated since new information is actually being loaded into the buffer.

7.5.1.2 Output Instructions

- AG X.Y.2 Output operating mode bits

  Bit 1 Stop

  Switch off motor and switch on reader coupling (the read process stops).

  Bit 12 Start

  Output motor and reader coupling (reader starts).

7.5.2 Interrupt Release

An interrupt is released when the buffer contains new data which can be transmitted to the system.

7.5.3 Addressing

The I/O 1801 is used for addressing purposes (see Section 7.1).

7.6 I/O Assignment for Tape Punch 0090.00

7.6.1 Description of I/O Assignment

The tape punch is connected to the I/O 1801 via cable 7034.

One input instruction and one output instruction are required to operate the tape punch.

7.6.1.1 Input Instructions

- EG X.Y.3 Interrogate tape punch status bits.

  Bit 9 Tape punch timing

  This bit is set when a punch process is taking place. When it is not set the next item of punch information can be outputted.

Bit 10 Pilot hole

This bit is required when processing edge punched cards. It signals the end or beginning of an edge punched card.

Bit 11 Not used

Bit 12 End of paper, punch fault

This bit is set when the feed spool is empty or when the take-up spool is full.

7.6.1.2 Output Instructions

- AG X.Y.1 Output punch information

Bits 1 to 8 Output punch information

Bit 9 Release

The coupling magnet is addressed, bit 9 must always be outputted in conjunction with bits 1 to 8.

7.6.2 Interrupt Release

The tape punch is interrupt-controlled. Interrupt release is via the "tape punch timing" signal (bit 9 of EG X.Y.3).

7.6.3 Addressing

See Section 7.1.

7.7 I/O Assignment of the 1801 when used to Control Mark Reader, Connected via Cable 7031

Row \ Bit	12	11	10	9	8	7	6	5	4	3	2	1
EG Y.1					Doc. Reject	Doc. Present	no inter-rogation	Read Window	stacker	Doc. Ready	WT 2	WT1
Signal path					A36, La7	A31, La3	A26, La5	A21, La4	A16, La9	A11, La8	A6, La2	A1, La1
EG Y.2					Line Reject	Doc. Vor.	ML fault		K20	K19	K18	K17
Signal path					A37, La6	A32, Lc11	A27, La12		A17, Lb10	A12, Lb9	A7, Lb8	A2, Lb7
EG Y.3					K16	K15	K14	K13	K12	K11	K10	K 9
Signal path					A38, La6	A33, Lb5	A28, Lb4	A23, Lb3	A18, Lb2	A13, Lb1	A8, Lc10	A3, Lc9
EG Y.4					K 8	K 7	K 6	K 5	K 4	K 3	K 2	K 1
Signal path					A39, Lc8	A34, Lc7	A29, Lc6	A24, Lc5	A19,Lc4	A14, Lc3	A9, Lc2,	A4. Lc1
AG Y.1									Select 2	Select 1	Read	Feed
Signal path									A75	A71,Lb11	A66, La10	A62, La11
AG Y.2												
Signal path												
AG Y.3												
Signal path												
Interrupt					4 B	4 A	3 B	3 A	2 B	2 A	1 B	1 A
Signal path											A69, La5,7	A64

7.7.1 Description of I/O Assignment

Four input instructions and one output instruction are required to operate the mark reader.

7.7.1.1 Input Instructions

- EG X.Y.1 Interrogate status bits

  Bits 1 and 2 — WT 1/WT 2

  Signals for line change

  Bit 3 — DOC READY

  This signal denotes that a document is present at the read station, CPS.

  Bit 4 — STACKER

  This signal is transmitted when the stacker is full or the hopper is empty.

  Bit 5 — READ WINDOW

  Duration of data transmission.

  Bit 6 — No interrogation

  The information in channels 1 to 20 is not binding.

  Bit 7 — DOC. PRESENT

  The document in question remains at the read station for the duration of this signal (length of document).

  Bit 8 — DOC. REJECT

  This signal is transmitted when there is a timing track defect or when a document being read is not straight.

- EG X.Y.2 Interrogate information and status bits.

  Bits 1 to 4 — Channels 17 to 20

  Information lines

  Bit 6 — Error lamp

Bit 7 DOC VOR (START 1)

Feed document as far as rocker 1.

Bit 8 LINE REJECT

This indication is given for each line if marks are too faint.

- EG X.Y.3 Interrogate information bits

Bits 1 to 8 Channels 9 to 16

Information lines

- EG X.Y.4 Interrogate information bits

Bits 1 to 8 Channels 1 to 8

Information lines

7.7.1.2 Output Instructions

- AG X.Y.1 Output operating mode bits

Bit 1 FEED

Feed document from separator, document remains at CPS.

Bit 2 READ

Read document in marker reader.

7.7.2 Interrupt Release

The mark reader is interrupt-controlled and and interrupt is released each time an information item is read. In addition the signal DOC. REJECT releases an interrupt.

7.7.3 Addressing

See Section 7.1.

8 I/O 1802

The I/O is used to control the magnetic disks.

8.1 I/O Assignment

- Input assignment

Row \ Bit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
EG 0.0.0.0.0									← IR number							→
EG 0.0.X.0.1						parity error	output error	KSTP	FBNR	FSNR	LODA	NAP1	FB	sync error	COMP error	check character error
EG 0.0.X.2.1 drive no. 0									400 SP	split	First Seek	air pressure present	ready	error	seek error	end of pos.
EG 0.0.X.2.2 drive no. 0										Strobe	2200 bpi	← sector counter				→
EG 0.0.X.2.5 EG 0.0.X.2.6 drive no. 1																
EG 0.0.X.2.9 EG 0.0.X.2.10 drive no. 2																
EG 0.0.X.2.13 EG 0.0.X.2.14 drive no. 3																
≈	≈															
EG 0.0.X.3.13 EG 0.0.X.3.14 drive no. 7																

Output assignment

Row \ Bit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AG 0.0.0.0.0	IR limit number								IR limit number							
AG 0.0.X.0.0					0				interrupt number							0=enable
AG 0.0.X.0.0					1											1=disable
AG 0.0.X.0.1	FAR 1 ... FAR 16															
AG 0.0.X.0.2	FLZ [(n's complement −1)															
AG 0.0.X.0.3							FAR20	FAR19	FAR18	FAR17		SZR				
AG 0.0.X.2.0					1										0	0-delete
															0	1-INT
															1	0-DMA
AG 0.0.X.2.1 drive no. 0								track difference (n's complement)								
AG 0.0.X.2.2 drive no. 0									forward	current reduction	Restore	here bit 5 is decimal and not hexadecimal head address				
AG 0.0.X.2.3 drive no. 0							FKPOS	FAGOD	FAGOS	wind forward without SYN	MI	2,5 MHz	18 Bit	LMVG	write	read
AG 0.0.X.2.5 drive no. 1																
AG 0.0.X.2.6 drive no. 1																
AG 0.0.X.2.7 drive no. 1																
AG 0.0.X.3.13 drive no. 7																
AG 0.0.X.3.14 drive no. 7																
AG 0.0.X.3.15 drive no. 7																

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8.1.1 Description of I/O Assignment

There are 4 input and 9 output instructions for the I/O 1802.

8.1.1.1 Input Instructions

- EG 0.0.0 Interrogate interrupt number
- EG X.0.1 Interrogate status bits

Bit 1 CC comparison (CC comp.)

Bit 1 is set if the check character formed during a read operation differs from the check character read out from the track by the preceding read operation.

Bit 2 Read and compare error (LVG)

Bit 2 is set if the data read from a disk differs from the previously entered data during operation in the "read and compare" mode.

Bit 3 Synchronizing character not detected (SYN error).

Bit 3 is set if the synchronizing bit was not detected during a "read" operation with a specified time Δ t after the reception of the required sector pulse (enable write permit).

Δ t for 1.25 and 2.5 MHz operation = 200 us.

The read operation is truncated and the I/O 1802 is cleared when a SYN error occurs.

Bit 4 Busy flip-flop

"Busy flip-flop" is set by the output instruction start (AG X.Y.3*) and can be restored by the following conditions:

a) When data traffic is completed normally (stop).

With the following causes of faults:
Incorrect sector number
Incorrect block number
LOST DATA
SYN error
No stop
Peripheral device power failure

b) When a positioning error is detected

* X = 1802 board address, Y = station address (2 for station 0)

Bit 5 Power failure in peripheral device (NAP 1)

Bit 5 is transmitted if there is a power failure in a peripheral device. (Power failure in one of the connected magnetic disk stations.)

Bit 6 LOST DATA (LODA)

Bit 6 is set if an old I/O cycle runs when an I/O backplane request is made, i.e. when the cycle-stealing mode malfunctions. When this happens data exchange is terminated by the clear board signal.

The error message RU is included in the error message LODA, i.e. LODA is also set if RU is still present at the backplane after a period of 20 us because of a cycle fault.

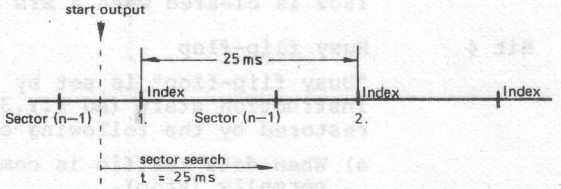
The I/O 1802 is reset by LODA and the RU of the I/O 1802 is removed from the backplane.

Bit 7 Incorrect sector number (FSeNr)

Bit 7 is set if the desired sector is not detected within the period required to detect 2 index pulses (transfer of incorrect sector numbers).

Sector numbers are continuously transmitted from the addressed magnetic disk station (0564) to the sector counter register of the I/O 1802.

Worst case waiting time corresponds to the time taken for a disk to complete one rotation, i.e. 25 ms.



Bit 8 — Incorrect block number (FBINr)

Bit 8 is set if the I/O unit addresses a memory plug-in unit which is defective or is not present.

The criterion adopted is that within a specified waiting time (10 us approx.), which is greater than the access time of the memory, the memory start signal must be followed by a strobe reply signal. If this requirement is not fulfilled data exchange in the I/O unit is truncated by the board clear signal.

Bit 9 — No stop

Bit 9 is set if the index mark is overrun twice during the exchange of data. Such a fault originates in hardware and can occur if the stop signal, which should terminate normal exchange of data, is not generated or is ineffective. A magnetic disk which has already been started would not reply given such a hardware fault.

The I/O 1802 is also cleared in this case.

Bit 10 — Output error (AG-error)

Bit 10 is set if an illegal output instruction (i.e. AG FAR, AG FLZ) is outputted on the I/O 1802 when the "busy flip-flop" /FB) bit is set.

All output instructions are illegal except the following:

The head address register (KAR) or the track difference counter (SPD) of a magnetic disk in which no exchange of data is taking place may be loaded. This enables other magnetic disk units to be positioned during the exchange of data (simultaneous mode).

If outputs are transmitted to the head address register or track difference counter of a magnetic disk unit in which exchange of data is taking place, these outputs will be identified as errors.

The I/O 1802 reacts to illegal outputs as follows:

a) The output instruction is received but is ineffective.

b) Bit 10 is set.

Bit 11 Parity error

Bit 11 identifies the reception of a byte from the backplane containing a parity error (this is only possible during "read and compare" or "write" in the 16-bit operating mode).

Conclusion With the exception of "busy flip-flop" (FB) all error indicators are set when the error in question occurs, and are reset when the next output instruction is outputted.

The errors LODA, FSeNr, SYN-fault, NAP 1 and no stop also immediately clear the I/O 1802 as well as the "busy flip-flop" signal. The I/O 1802 is also cleared when the NA signal is detected in the repeat mode.

- EG X.2.1 Interrogate status bits for magnetic disk station 0.

Bit 1 End of positioning

Bit 1 is set when a positioning operation has been completed.

Bit 2 Positioning fault

Bit 2 is set if a positioning operation has not been completed within one second.

Bit 3 Error

Bit 3 is set if any of the following errors are detected in the 0564.xx: Incorrect voltage, speed error, head selection error or an error during a write or read operation (see description of the 0564.xx).

Bit 4 Ready

Bit 4 is set when the magnetic disk station is ready to operate.

Bit 5 Air pressure present

Bit 5 is set when the magnetic disk station air pressure is present.

Bit 6 First-seek

Bit 6 is set when a first-seek (first positioning after switching on) has been carried out.
Bit 6 is reset when the next restore instruction is outputted.

Bit 7 Split

Bit 7 is set when a split magnetic disk station is used.

Bit 8 400 SP

Bit 8 is set when a 60 million byte magnetic disk station is used (60 million bytes = 400 cylinders).

8.1.1.2 Output Instructions

- AG X.0.0 Output interrupt number

  Bit 12 = "0": The interrupt number to be outputted is in bits 1 to 8.

  Bit 12 = "1": Bit 1 determines whether the I/O is disabled or enabled for interrupt operation.

  Bit 1 = "1": Interrupt disable

  Bit 1 = "0": Interrupt enable

- AG X.0.1 Load the field address register

  Output address bits 1 to 16.

- AG X.0.2 Load the field length counter

  The field length is outputted as n complements - 1.

- AG X.0.3 Output sector number and address bits 17 to 20 for the field address register.

  When sector number is outputted the sector being sought must be outputted as - 1.

- AG X.2.0 I/O 1802 output instructions for test purposes

  Bit 12 = "1"
  Bit 1 = "0"
  Bit 2 = "0"
  } Clear instruction for the I/O 1802

  Bit 12 = "1"
  Bit 1 = "1"
  Bit 2 = "0"
  } Releases an interrupt in the I/O 1802

  Bit 12 = "1"
  Bit 1 = "0"
  Bit 2 = "1"
  } Releases the DMA cycle in the I/O 1802

- AG X.2.1 Output the track difference for magnetic disk station 0.

  The "track difference" is outputted as an inverted statement (complement).

- AG X.2.2 Output magnetic disk related data

  Bit 1 to 5 Head address

  Bit 5 is decimal and not hexadecimal.
  Examole: Output head 14 = 1.4,
  Output head 10 = 1.0 etc.

  Bit 6 Restore

  Bit 7 Current reduction

  From cylinder 128 with GA 1 and 3 and cylinder 256 with GA 0.

  Bit 8 Positioning direction

  Bit 8 = "1": backwards
  Bit 8 = "0": forwards

- AG X.2.3 Output operating mode bits

  Bit 1 Read

  Bit 2 Write

  Bit 3 Read and compare

  Bit 4 Changeover bit for 16-or 18-bit operation

  Bit 4 = "0": 16-bit operation
  Bit 4 = "1": 18-bit operation

Bit 5 Changeover bit for write or read frequency

Bit 5 = "0": Bit frequency 1.25 MHz (1100 bpi)
Bit 5 = "1": Bit frequency 2.5 MHz (2200 bpi)

Bit 6 Changeover bit for type of memory

Bit 6 = "0": working memory
(If bit 4 = "0" bit 6 is not evaluated i.e. a main memory is being addressed).

Bit 6 = "1": micromemory

Bit 7 Write leader tape without SYN-Byte

The SYN Byte is replaced by a Null Byte. In conjunction with write (Bit 2) a whole track can be erased, i.e. entered as nulls.

Bit 8 Start FAGOS

Data exchange without end of positioning interrogation and sector search.

Bit 9 FAGOD sector search without data exchange

For test purposes only.

Bit 10 FKPOS Start of sector search without previous end of positioning interrogation.

8.2 Interrupt Release for Magnetic Disk Data Processing

The resetting of FB also serves as an interrupt release; this sets an interrupt message flip-flop. In addition each error bit which is set, except bit 11 (CC error) and bit 2 (LVG) releases an interrupt.

8.3 Addressing

- Address bit assignment

Bits
1 and 2 I/O line number

Bits 3 to 5 Magnetic disk unit number (if bit 6 = "1")

Bit 6 If bit 6 = "0" all registers, which can be loaded or interrogated independently from the magnetic disk unit number, are addressed (i.e. only the register of the I/O 1802).

If bit 6 = "1" all registers, which can only be loaded or interrogated depending upon the magnetic disk unit number, are addressed.

(For exception see AG 0.0X.2.0)

Bits
1 to 11 I/O 1802 address

Bit 12 Bit 12 = "1" for all output instructions.

Bits
13 to 18 Contain "0" when the I/O is being addressed.

NIXDORF COMPUTER Kundendienst

9 DMA 1804

The DMA is used to control high-speed peripheral devices.

9.1 I/O Assignment

Instruction \ Bit	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
EG 0.0.0.0											interrupt number register							
EG X.0.2											original character register							
EG X.0.3							block length counter											
EG X.0.4							special chars.	BLZO	FVPD DY	FZDP DY		FVPD DE	FZDP DEA	BLEN	time error mem.	VPC error mem.	end of area not r.	over-flow
EG X.0.8 – EG X.15.15							dynamic input											
AG X.0.0							disable and enable INT no. 1 0				interrupt number register							dis.=1 en.=0
AG X.0.1			block address counter															
AG X.0.2												group selection block address			block address counter			
AG X.0.3							block length counter											
AG X.0.4			start of code table register															
AG X.0.5												group selection code table			code table register			
AG X.0.6							INT for code 0	INT for BLZ				SSP	count back-wards	data transp. despite PAINT	read mem. off	format change		
AG X.0.7							delete special chars.	delete BLZO	delete FVPD	delete FZDP	ZUP off	delete DMA						
AG X.0.8 – AG X.15.15							dynamic output											
AG 0.0.0.0.0.			complete limit number								limit number							

9.1.1 Description of I/O Assignment

DMA Input and Output instructions.

9.1.1.1 Input Instructions

- EG X.0.0 — Interrogate the interrupt channel number.
- EG X.0.2 — Read in the content of the original character register.

  the original code of a character is entered in the original character register if null (= special character) is detected when working with the DMA internal code transcription when a character code has been transcribed.
- EG X.0.3 — Read out the content of the block length counter register.
- EG X.0.4 — Read the status of the markers (status details).

  Bit 1 — Overflow (BÜ)

  If bit 1 is set more characters were received than were indicated in the block length counter. The number of extra characters received is present in the block length counter as a complementary value.

  Bit 2 — End of area not reached (BU)

  If the program loads the block length counter with a value bit 2 is set (start of DMA operation = independent data traffic).

  Bit 2 is reset, i.e. cleared, if the value of the block length counter is null when an input or an output operation has been completed.

  Bit 3 — VPC error memory (parity error)

  Bit 3 is set if a parity error is detected during a DMA memory cycle. The DMA operation which is running is truncated.

  Bit 4 — Time error memory

  Bit 4 is set if a time error is detected during a DMA memory cycle. The DMA operation which is running is truncated.

Bit 5 BLEN (negated block length end generator)

Bit 5 is set when the block length counter is loaded.

Bit 5 is deleted when a DMA input or output operation has been satisfactorily completed on the PSP end, i.e. for an input the block length end signal is detected on the PSP or, for an output, the block length counter is null.

Bit 11 = "1": BLZO block length counter equal to null.

Bit 6 FZDPDEA (error message for time error in DMA and peripheral device during data input or output).

Bit 6 is set if a time fault is detected in the PSP during DMA data transmission (input or output) between DMA and peripheral device. Time monitoring = 10 us.

Bit 7 FVPDDE (error message or VPC parity error in peripheral device and DMA during data input).

Bit 7 is set if a parity error is detected in the PSP during DMA data traffic (input) between peripheral device and DMA.

Bit 8 Not used

Bit 9 FZDPDY (error message for time error in DMA and peripheral device during a dynamic input or during interrupt interrogation of peripheral device).

(Dynamic input or output is equivalent to input or output controlled by the central processing unit).

Bit 9 is set if a time error is detected in the PSP during a dynamic input or output or during interrupt number interrogation of peripheral device (by means of the instruction EG 0).

Bit 10 FVPDDY (error message for VPC parity error in peripheral device and DMA during dynamic input or during interrupt interrogation of peripheral device).

Bit 10 is set if a parity error is detected in the PSP during dynamic input or during interrupt number interrogation of peripheral device.

Bit 11 BLZO (interrupt flag for block length end).

Bit 11 is set if the block length counter assumes the value null during DMA traffic (output). When bit 11 is set this can release an interrupt if required, provided that bit 11 was previously outputted on AG 6.

Bit 12 Special character bit

Bit 12 is set, during DMA traffic, the information null is detected after code transcription. The code of the original character is stored in the original character register.

When bit 12 is set this can release an interrupt if required, provided that bit 12 was previously outputted on AG 6.

9.1.1.2 Output Instructions

- AG X.0.0 This instruction loads the interrupt register.

  Bit 12 and 11 = "0": The interrupt number is outputted in bits 1 to 8.

  Bit 12 = "1" and Bit 11 = "0": Bit 1 determines whether the interrupt is inhibited (Bit 1 = "1") or enabled (Bit 1 = "0")

- AG X.0.1 Load the block start address counter register.

- AG X.0.2 This determines with which type of memory (HA, Mi or AR) the DMA communicates:

  Bit 5 = "1": Micromemory (Mi)
  Bit 6 = "1": Working memory (AR)
  Bit 7 = "1": Main memory (HA)

- AG X.0.3 Load the block length counter register.

  This instruction simultaneously instructs the DMA to initiate automatic data transmission.

- AG X.0.4 Load the start of code table register.

- AG X.0.5 This instruction determines in which memory the code table is located.

  Bit 5 = "1": Micromemory (Mi)
  Bit 6 = "1": Working memory (AR)
  Bit 7 = "1": Main memory (HA)

- AG X.0.6 Set the operating mode flip-flops

  Bit 1 = "1":
  Bit 2 = "0": } 2 x 8-bit data format
  Bit 3 = "0":

  Bit 1 = "0":
  Bit 2 = "0": } 1 x 12-bit data format
  Bit 3 = "0":

  Bit 1 = "1":
  Bit 2 = "1": } 2 x 8-bit data format with code transcription
  Bit 3 = "0":

  Bit 4 = "0": Data transfer is from the peripheral device to the memory.

  Bit 4 = "1": Data transfer is from the memory to the peripheral device.

  Bit 5 = "1": Data transfer is not interrupted by any parity errors which may occur.

  Bit 6 = "0": Count forwards for data transfer, i.e. lowest address first.

  Bit 6 = "1": Count backwards for data transfer, i.e. highest address in buffer first.

  Bit 7 = "1": The supply voltage (24V/0V) is taken from the peripheral interface of the DMA.

  Bit 11= "1": If the content of the block length counter register has become null, an interrupt request is outputted to the central processing unit.

  Bit 12= "1": If the value null (special character) is read during code transcription an interrupt request is outputted to the central processing unit.

- AG X.0.7 Delete status flags

  Bit 7 = "1": DMA system reset.

  Bit 8 = "1": The 10 us time monitoring for data transfer between the peripheral device and the DMA is turned off.

  Bit 9 = "1": Delete time error status message.

  Bit 10 = "1": Delete parity error status message.

  Bit 11 = "1": Delete block length counter null status message.

  Bit 12 = "1": Delete special character status message.

9.1.2 Inter-Relationship Between the Content of the Block Length Counter and Status Register Bits 1, 2, 3, 4, 5, 6, 7, 11 and 12

Bits 2 (BU) and 5 (BLEN) are set to "1" when the block length counter is loaded.

- Final states after completion of DMA operation

  - Block length counter equals null, bit 2 (BU) and bit 5 (BLEN) deleted, all other status bits except bits 9 and 10 deleted.

    The DMA input operation called up was completed correctly.

    Bits 9 and 10 relate to the dynamic operating mode, i.e. they are irrelevant as far as DMA operation is concerned.

  - Bit 11 (BLZO) set, bit 5 (BLEN) and bit 2 (BU) deleted, block length indicator equals null, no other status bits set.

    The DMA output operation called up was completed correctly.

  - Block length counter not equal to null, bit 5 (BLEN) not set, bit 2 (BU) set, no other status bits set.

    The DMA input operation called up was completed correctly, although the end of area was not reached, i.e. the program envisaged more input characters than were provided by the peripheral device. The number of characters which were not received is present in the block length counter.

- Block length counter not equal to null, bit 5 (BLEN) not set, bit 2 (BU) not set, bit 1 (BU) set, not other status bits set.

  The DMA input operation called up was completed correctly, but there was overflow. There is overflow when an input from the peripheral device transmits more characters to the DMA than was envisaged by the program. A statement of the number of extra characters which were received is present in the block counter in inverted form. The extra characters which were transmitted are lost.

- Block length counter not equal to null, bit 5 (BLEN) set, bit 2 (BU) set, bit 3 or 4 (VPC or time fault) set, no other status bits set.

  The DMA input or output operation called up was not completed correctly and was truncated. This was due to the parity or time fault memory.

  The number of characters which are to be received or to be transmitted is present in the block length counter.

- Block length counter not equal to null, bit 2 (BU) set, bit 5 (BLEN) set, bit 6 or 7 (FZDPDEA or FVPDDE) set, not other status bits set.

  The DMA input or output operation called up was not completed correctly and was truncated. This was due to time faults or parity errors in the magnetic disk store.

  The number of data items which are to be transmitted or received is present in the block length counter.

- Block length counter not equal to null, bit 2 (BU) not set, bit 5 (BLEN) set, bit 1 (BU) set, bit 6 or 7 (FZDPDEA or FVPDDE) set, no other status bits set.

  The DMA input operation called up was not completed correctly and was truncated. This was due to time errors or parity errors in the PSP. There was also overflow.

  A statement of the number of extra characters received is present in the block length counter in complementary form.

- Bit 9 (FZDPDY) or bit 10 (FVPDDY) set; other status bits can be set as required, since simultaneous operation is permitted between DMA operation and dynamic operation.

  A time error or a parity error was detected in the PSP when a dynamic input or output instruction was made.

  At the time of writing bit 12 is not used.

- Delete status bits

  Status bits 9, 10, 11 and 12 must be deleted for each output instruction (AG 7).

  Note: Bits 9 and 10 are not always reset after a fault has occurred, care must therefore be taken in the evaluation of these bits.

  The other status bits are reset by the interrogation instruction EG 4.

9.2 Interrupt Release in DMA

Interrupts can be released by bit 11 (BLZO) and bit 12 (special character).

With BLZO = "1" it is therefore possible to signal the end of DMA output operation by an interrupt release (this must, however, have been determined previously by outputting bit 11 on AG 6).

At the time of writing interrupt release by means of recognition of special characters is not used.

The system is not informed of the completion of a DMA operation by the release of a DMA interrupt. If the end of an input operation is signalled by an interrupt then it is an interrupt from an external peripheral device.

9.3 DMA Addressing

The DMA address used at the time of writing is 6.0.X.

X = input or output line

10 DMA Header 5000

The DMA feature constitutes the connection between the DMA 1804 and the tape control unit.

10.1 I/O Assignment of the Magnetic Tape Control Unit

Row / Bit	8	7	6	5	4	3	2	1
EG 0.0 device information adr.	IE 8	IE 7	IE 6	IE 5	IE 4	IE 3	IE 2	IE 1
EG 0.1 read data	Inf. 8	Inf. 7	Inf. 6	Inf. 5	Inf. 4	Inf. 3	Inf. 2	Inf. 1
EG 0.0 + GA Status 0							NRZI/PE device	9/7 channel
EG 0.1 + GA Status 1	NA(FF)	PF(FF)	TEMP		CERS (FF)	DATAER (FF)	ZTF (FF)	REJECT (FF)
EG 0.2 + GA Status 2		IDENTS (FF)	BOT	FPT	RWD	RDY	FM (FF)	EOT (FF)
EG 0.3 + GA Status 3					D-BUSY	C-BUSY		
AG 0.1 write data	Inf. 8	Inf. 7	Inf. 6	Inf. 5	Inf. 4	Inf. 3	Inf. 2	Inf. 1
AG 0.0 + GA device information adr.	IA 8	IA 7	IA 6	IA 5	IA 4	IA 3	IA 2	IA 1
AG 0.1 + GA instructions	← encoded instructions (see list of instructions) →							
AG 0.2 + GA instructions							JVLN	JVSN

GA = device address

10.1.1 Description of I/O Assignment

There are 4 input instructions and 3 output instructions.

Inputs EG 01. and output AG 0.1 relate exclusively to independent DMA transfer.

EG 0.1 = Input data characters for independent operation.
AG 0.1 = Output data characters for independent operation.

10.1.1.1 Input Instructions

- EG 0.0 — Interrogate the interrupt number of the magnetic tape control unit.

- EG 0.0+GA — Interrogate the status bits of status line 0.

  Bit 1
  "0" = channel 9
  "1" = channel 7

  "1" = PE device
  "0" = NRZI device

- EG 0.1+GA — Interrogate the status bits of status line 1.

  Bit 1 — REJECT (FF) instruction not accepted.

  This state is set if an instruction from the magnetic tape control unit is not accepted.

  The following conditions entail REJECT:

  a) The magnetic tape control unit is still working and receives a new instruction (except OST).

  b) Rewind instruction received when the device is at BOT.

  c) Write instruction without write entry.

  d) Invalid instruction code.

  Bit 2 — ZTF (FF) time error

  This state indicated that, during data transfer between the magnetic tape control unit and the magnetic tape station, information was not accepted on time by the receiver (e.g. because of incorrect start stop time).

Bit 3 DATA ER (FF) check character error

This state indicated that an error was detected during read or check read for a write operation.

in NRZI	in PE
VPC error	correctable error (CERS-"1")
LPC error	incorrectable error (CERS-"0")
or	defective preamble or postamble
CRC error	skew failure or
	drop out on more that one track

Bit 4 CERS (FF) single error corrected

This state only applies to PE devices during read operations. It indicates that there was a single error which was automatically corrected.
A single error means that a 1-bit error correction was made in a data character (bit added automatically).

Bit 6 TEMP (temperature error)

"1" = the internal temperature of the device is too high.
Although this state does not affect readiness to work it can however, lead to information errors if the device continues to be operated.

Bit 7 PF (FF) parity error

"1" = there was a parity error in the magnetic disk store in an information cycle or in a data cycle.

Bit 8 NA (FF) power failure

"1" = the power pack of the magnetic tape control unit has reported NA.

• EG 0.2+GA Interrogate status bits of status line 2

Bit 1 EOT (FF) end of tape mark

"1" = end of tape mark detected.

Bit 2 FM (FF) tape mark detected.

Bit 3 RDY ready to operate

"1" = the device addressed is on REMOTE and is ready to accept an instruction.

Bit 4 RWD rewind status

"1" = the device is rewinding and has not yet reached BOT.

Bit 5 FPT reel write enable ring

"0" = no write enable ring on rel. No write entry can be made.

Bit 6 BOT beginning of tape mark

"1" = the tape is at BOT.

Bit 7 IDENTS (FF) PE indentification block detected.

"1" = PE identification block detected during the first read instruction (first time tape is addressed).
The tape in question has already been written on by the PE.

- EG 0.2+GA Interrogate the status bits of status line 3.

Bit 3 CBUSY magnetic tape control unit activated.

"1" = an instruction is being dealt with in the magnetic tape control unit.

Bit 4 DBUSY write or read status

"1" = the magnetic tape control unit is dealing with the part of an instruction sequence in which data is being written or being read.

10.1.1.2 Output Instructions

- AG 0.0+GA — Load the interrupt register of the magnetic tape control unit (the interrupt number must be in bits 1 to 4).

- AG 0.1+GA — Output encoded magnetic tape control unit instructions.

  List of instructions for the magnetic tape control unit.

Abbreviation	Description	Code
DBS	Write a data block	4.1
DBLV	Read a data block forwards	2.1
DBLR	Read a data block backwards	2.2
BS	Write a tape mark	4.2
DBV	Unwind one data block	2.7
DBR	Rewind one data block	1.1
GV	Run forward 64 mm with erase	4.4
RW	Rewind to beginning of tape mark	1.2
RWL	Rewind to beginning of tape mark and switch off	1.4
LV	Changeover read threshold	0.3
UP	Changeover parity bits	1.7
DDS	Changeover bit density	2.4
OST	Stop operation	0.0

- AG 0.2+GA — Output for interrupt inhibit or interrupt enable.

  Bit 1 — IVSN

  Implement interrupt lock.

  Bit 2 — IVLN

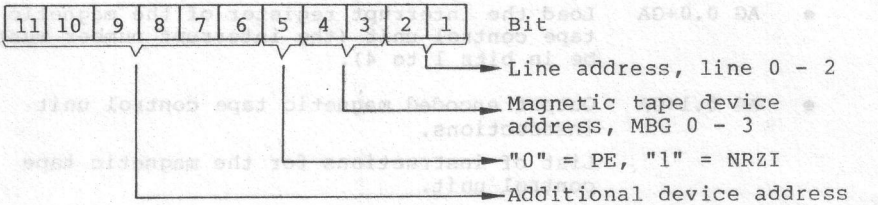
  Delete interrupt lock.

10.2 Interrupt Release

Each instruction, except "rewind" and "rewind and switch off", is terminated by an interrupt.

The interrupt line can be disabled or enabled by means of the instructions "set interrupt lock" (IVLN) and "reset interrupt lock" (IVLN).

10.3 Addressing



11 DMA Header 0411.01

The DMA feature connects the DMA 1804 and card reader 0491.01 or 0492.01.

11.1 I/O Header Assignment

Row \ Bit	8	7	6	5	4	3	2	1
EG 0.0	interrupt address							
EG X.Y.1	parity error	multi-punching	ERROR	HOPPER CHECK	MOTION CHECK	READY	start read cycle	
EG X.Y.2	information from channel amplifier via DMA to CPU							
EG X.Y.3	read timing	Busy	row 3	row 2	row 1	row 0	row 11	row 12
EG X.Y.4	column counter 0		row 9	row 8	row 7	row 6	row 5	row 4
EG 0.1	information from channel amplifier to the DMA							
AG X.Y.0	interrupt address							
AG X.Y.1	0	L=number of columns to be transmitted						
AG X.Y.2	0	K=last column before window						
AG X.Y.3	0	I=last column of a window						
AG X.Y.4	Pick-Command	check interrupt	mark reader	binary data transmission	delete instruction	start transmission	start read	interrupt disable

11.1.1 Description of I/O Assignment

There are 5 input instructions and 5 output instructions.

11.1.1.1 Input Instructions

- EG 0.0.0 — This is an instruction to interrogate the interrupt number of the feature.

- EG 0.1 — This input line transmits data located in the buffer via the DMA to the CPU (independent transfer). This line cannot be addressed via dynamic instructions.

- EG X.Y.1 — Interrogate reader status bits

  Bit 2 — Start read cycle

  This bit is set when "start read" is outputted. It is deleted by the dynamic input instruction EG X.Y.1, after the end of data transmission interrupt, by a power failure in the card reader or by outputting "clear buffer". If the flag is deleted because of a power failure, the last card transported must be replaced.

  Bit 3 — READY

  This bit indicates that the card reader is ready to operate and respond to a card transport instruction. This bit is reset by a power failure or a fault in the card reader.

  Bit 4 — MOTION CHECK

  This bit indicates a transport fault. Either card n could not be transported or card (n-1) could not be stacked properly. This signal is cleared by a power failure.

  Bit 5 — HOPPER CHECK

  This bit either indicates that the hopper is empty or the stacker is full. Do not replace any cards.

Bit 6 — ERROR

This bit is set if an error is detected at the beginning and the end of a card when it is being read during light/dark checking. The card in question must be replaced and read again. This signal is cleared by a power failure.

Bit 7 — Multi-punching

This bit is set if more than one hole is detected in rows 1 to 7 of a column of a card. The setting of this marker is suppressed during binary data transmission and for a single window mask. This flag is deleted by the next dynamic EG X.Y.1 instruction or by a power failure.

Bit 8 — Interface parity error

The "parity error" flag is set if, during transmission from the DMA to the card reader DMA feature, a parity error is detected in an information cycle. In addition the signal QUITT (acknowledge) is not switched. The DMA will therefore detect a time fault. If a parity error is detected in an address cycle only the QUITT (acknowledge) signal is not switched.

- EG X.Y.2 — Information from a card which has been read is present in the DMA feature buffer and can be read into the CPU dynamically via the DMA. In this case no interrupt is released for the end of data transmission.
It is also possible to initially transmit a few columns dynamically and transmit the remainder by independent data transfer.

- EG X.Y 3 and 4 — The 12 information lines of the card reader can be interrogated by means of input lines 3 and 4 (bits 1 to 6).

Bit 7 on EG 3 — This bit denotes the state of the card reader BUSY signal.

Bit 8 on EG 3 — This bit changes its state from index mark to index mark when a card is being read.

Bit 8 on EG 4 — Column counter

Bit 8 is set when the card reader DMA feature column counter is null.

11.1.1.2 Output Instructions

- AG X.Y.0 — Load the interrupt register of the DMA feature (the interrupt number must be in bits 1 to 4).

- AG X.Y.1 — Output the number of columns to be transmitted from the DMA feature buffer to the CPU.

- AG X.Y 2 and 3 — The location of a window which is to be blanked (e.g. microfilm window) can be defined by the following outputs:

  AG 2: K = last column before the window

  AG 3: I = last column of the window with K not greater that 80 and I not greater than 80.

- AG X.Y.4 — Output the operating mode bits

  Bit 1 — Interrupt channel inhibit

  The release of interrupts by the card reader DMA feature can be inhibited by outputting bit 1 = "1". All other functions remain unaffected.

  Bit 2 — Start read

  Outputting this bit initiates the reading of a card, provided that the card reader is in the READY operating state. Card information is transmitted to the header buffer. "Start read" for the next card does not occur until the "end of read" interrupt has been processed.

  Bit 3 — Start transmission

  When this bit is outputted the card reader DMA feature starts automatic data transmission with the DMA. The specified number of column information items (output on AG 1) is transmitted to the CPU.

  Bit 4 — Clear instructions

  The contents of the buffer is invalidated when this bit is outputted. The flag multi-punching, start, read cycle, read timing, interrupt inhibit, parity error information, column counter, window registers and FF interrupt flags are cleared and reset. A new read cycle can now be started.

Bit 5 Binary data transmission

Data is transmitted in binary form when this bit is outputted. Data is transmitted in encoded form when this bit is not set.

Standard punched card, encoded

This operating mode is the most widely used. The information for one column is transmitted in 8 bits = 1 byte.
Lines 1 to 7 are encoded in binary form in bit 3, whilst the remaining 5 lines are outputted directly.

Bit 1: 2^0
Bit 2: 2^1 } Lines 1 to 7 encoded
Bit 3: 2^2
Bit 4: Line 0
Bit 5: Line 11
Bit 6: Line 12
Bit 7: Line 9
Bit 8: Line 8

Standard punched card, binary

This operating mode is selected by setting bit 5 in output line 4. Each column is transmitted in two bytes. The flag "multi-punching" cannot be set.

Bit assignment for the two bytes:

Byte 1	Byte 2
Bit 1: Line 12	Bit 1: Line 4
Bit 2: Line 11	Bit 2: Line 5
Bit 3: Line 0	Bit 3: Line 6
Bit 4: Line 1	Bit 4: Line 7
Bit 5: Line 2	Bit 5: Line 8
Bit 6: Line 3	Bit 6: Line 9
Bit 7: 0	Bit 7: 0
Bit 8: 0	Bit 8: 0

Bit 6 Read marked cards

This bit must be outputted either before or at the same time that the instruction "start read" is outputted in order to inform the card reader DMA feature that marked cards are to be read. In this case the "end of read" interrupt is not requested immediately after the last index mark but 40 us max. after the card reader signal BUSY becomes "0". The maximum read speed of the card reader is also reduced.

Bit 7 Check interrupt

When this bit is outputted the card reader DMA feature requests an interrupt (in order to check the interrupt circuit).

Bit 8 Pick command

When this bit is outputted the transport of a card is triggered. Other functions of the card reader DMA feature remain unaffected.

All the bits of the output line 4 reset internally, with the exception of bit 1. Bit 1 can only be reset by the program.

11.2 Interrupt Release

An interrupt can be released either at the "end of read cycle" or at the "end of data transmission", provided that the interrupt inhibit has been cancelled.

11.3 Addressing

The address X.7.n is used at the time of writing.

X = DMA 1804 address = 6.0.0
n = Line address

12 Printer DMA Feature 4600

The printer DMA feature connects the DMA 1804 and the printer.

12.1 I/O DMA Feature Assignment

Row \ Bit	8	7	6	5	4	3	2	1
EG 0.0.0	← interrupt number →							
EG X.Y.1	check interrupt	automatic ready	Inf. Parity	end of feed	buffer empty		indicator	end of print
EG X.Y.2	parity error	automatic active	← printer identification →					
EG X.Y.3	Page	Load Image	Parity intern	feed	end of form	end of paper	indicator	printer request
AG X.Y.0	← interrupt number →							
AG X.Y.1	check interrupt	automatic ready	Inf. Parity	end of feed	buffer empty		indicator	end of print
AG X.Y.2	0	0	0	0	0	← operating char. * →		
AG X.Y.3	← characters to buffer →							
AG X.Y.4	← characters to printer →							
AG X.Y.5	← characters for automatic →							
AG X.Y.6	← number for automatic →							

*

Code	Function
0	Clear header buffer
1	Start DMA transmission
2	Start transmission from DMA feature to printer
3	Release check interrupt
4	Delete parity error
5	Clear DMA feature

12.1.1 Description of I/O Assignment

There are 4 input instructions and 7 output instructions.

12.1.1.1 Input Instructions

- EG 0.0.0 — Interrogate the interrupt number of the line printer DMA feature.

- EG X.Y.1 — Interrogate the interrupt cause bits.

  The 8 bits of this line indicate the reason an interrupt was released. This line is deleted as soon as the input instruction has been performed, and can therefore only be interrogated once for each interrupt from the line printer DMA feature. Interrogation can also be used to reset the markers.

  Bit 1 — End of print

  The end of print interrupt is always generated when the printer transmits its request signal and is ready to accept new characters as well as when the indicator is reset by the outputting of an end character.

  Bit 2 — Indicator

  The indicator interrupt is switched by the indicator signal from the printer (see status bit indicator).

  Bit 4 — Buffer empty

  The empty buffer interrupt is released when the independent transmission of characters from the DMA feature buffer to the hardware buffer of the printer has been completed.

  Bit 5 — End of feed

  The end of feed interrupt is released when the printer rejects the feed signal.

  Bit 6 — Information parity

  This interrupt is released when a parity error occurs in the PSP during block transmission. The line printer DMA feature truncates block transmission and the DMA indicates a time error.

Bit 7 — Automatic ready

The automatic ready interrupt is released when the automatic entry of characters (e.g. enter X blanks in the DMA feature buffer) has been completed.

Bit 8 — Check interrupt

This interrupt can be used to check the interrupt circuit and has no other significance of function.

- EG X.Y.2 — Interrogate printer identification and the status messages of the character printer DMA feature.

Bits 1 to 6 — Printer identification

These bits provide information concerning the wiring of the coding connector of the printer and enable the program to determine the type of printer (300, 600, or 1200 lines) and the character configuration of the print drum or print chain in question.

Possible printer identification:

0.0 or 0.2	Print mechanism with normal drum
0.3	Print mechanism with dual numerical drum

Bit 7 — Automatic active

This bit is set whilst the internal automatic equipment of the DMA feature is running. Since automatic operation is very rapid and the bit is present for a correspondingly short period of time, recognition is only possible from approximately 20 characters up.

Bit 8 — Parity error

This bit is set when an information parity error (hardware fault in the PSP) occurs during dynamic output instructions. This flag is deleted by the instruction "delete parity error".

- EG X.Y.3 — Interrogate printer status bits

Bit 1 — Request

The printer is ready to accept characters in its hardware buffer. When "request" is switched, indicator, end of paper and internal parity must not be set.

Bit 2 Indicator

The printer is not ready to operate because:

a) An illegal character or a character with incorrect parity was outputted.

In the following cases "indicator" can be deleted by the outputting of the end character. The printer is not triggered.

b) The paper has run out of the upper tractor and the printer is printing without paper.

c) The print member is swung off.

d) The channel tape reader is open.

e) A parity error has occurred in the hardware buffer of the printer.

Bit 3 End of paper

End of paper under the lower tractor.

Bit 4 End of form

Channel 12 on the channel tape has been detected. The flag is reset by the next end character that triggers a print.

Bit 5 Paper advancing

This bit is present as long as the paper is advancing.

Bit 6 Internal parity

A parity error has occurred in the hardware buffer of the printer. The indicator is set simultaneously. This flag can only be reset if the red reset button on the printer power pack is depressed or by switching the printer off and on. In this case wait approx. 10 seconds until the capacitors in the power pack have discharged.

CAUTION: The line printer DMA feature must subsequently be initialized once more.

Bit 7 Load image

This bit can only be set when using the chain printer, when the latter demands the image of the chain after switching on.

Bit 8 Page

Not used at time of writing.

12.1.1.2 Output Instructions

- AG X.Y.0 Load interrupt number (the interrupt number is in bits 1 to 4).

  The interrupt number is used to identify the device which is requesting the interrupt and is transmitted when the CPU is giving an EG 0.0.0 instruction and the DMA feature has interrupt priority.

- AG X.Y.1 Enable interrupt conditions

  "0" = Enable
  "1" = Disable

  All interrupts are disabled by switching-on clear, adapter clear or by depressing the red reset button on the printer power pack.

- AG X.Y.2 Output the operating characters

  Code 0 Clear DMA feature buffer

  The internal buffer address pointer is set to zero, i.e. the data which now follows will be placed in the buffer from address "null" onwards and, when printed, will therefore appear on the paper from position "null" onwards. Thus a new line is started.

  Code 1 Start DMA transmission

  The DMA must be prepared before this instruction is outputted i.e. the block length counter and the block address counter must be loaded.

  If a hardware parity error occurs in the PSP during block transmission, the line printer DMA feature truncates data transmission and releases an information parity interrupt. The DMA indicates a time error.

Code 2 — Start transmission from line printer DMA feature to the printer.

This instruction transmits the content of the DMA feature buffer to the hardware buffer of the printer. Only as many characters as were written into the DMA feature buffer after the last "clear DMA feature buffer" instruction are transmitted. The end of the transmission is reported by the "buffer empty". If the instruction "start transmission from the line printer DMA feature to the printer" is outputted again after a print operation has been performed, transmission takes place again. The contents of the DMA feature buffer is retained until it is written over.
Duration of transmission: 1.6 us per character.

Code 3 — Release check interrupt

This instruction releases an interrupt. It has no further effect.

Code 4 — Reset parity error flag

This instruction resets bit 8 in line 2 which is set by parity errors during dynamic output instructions.

Code 5 — Clear DMA feature

The line printer DMA feature acknowledges this instruction and clears itself, i.e. all registers are set to "null" and all interrupts are inhibited (as is the case after CPU deletion or switching on).

- AG X.Y.3 — Output character to the header buffer.

  This instruction writes the character located in the A register of the CPU into the DMA feature buffer after the characters already located in the DMA feature buffer. No check is made to determine whether the character is legal for printing purposes.

- AG X.Y.4 — Output character to the printer buffer

  This instruction writes in the character located in the A register of the CPU directly into the hardware buffer of the printer. The DMA and the line printer DMA feature function as normal I/O: The acceptance timing bit for the printer is formed by the line printer DMA feature hardware. The control characters for print release 0.12.2 (end character), for line feed 0.4.0 and channel feed 0.12.1 are also outputted on this line.

- AG X.Y.5 Output a character for the DMA feature register.

  This instruction loads a register in the line printer DMA feature with a character that is to be written into the DMA feature buffer automatically. This character remains in the register until it is written over.

- Ag X.Y.6 Output the number of characters for the DMA feature register.

  This instruction loads a counter in the line printer DMA feature and immediately writes in the inputted number of the loaded character into the DMA feature buffer with "character for automatic". The end message is by means of the "automatic operation ready interrupt". The number of characters can be between 0 and 255. (There is also an interrupt for the number "0").

  The instruction "start DMA" can be outputted even when an automatic operation is running. There is a lag and the line printer DMA feature starts the DMA as soon as the automatic is ready, provided that the DMA was prepared and the automatic ready interrupt is inhibited.

12.2 Interrupt Release While Operating the Printer

The end of each operational stage (automatic ready, end of transmission to the header buffer, end of transmission to the printer buffer, buffer empty, and end of print) is reported by an interrupt.

12.3 Addressing

The address X.6.n is used at the time of writing.

X = DMA address = 6.0.0
n = Line

For notes

13 I/O 1806

The I/O 1806 is used to control the line (V24 interface).

13.1 I/O Assignment

Row \ Bit	D3	D2	D1	8	7	6	5	4	3	2	1
EG Y.1	1		1	← input buffer →							
EG Y.2	0	1	0		← status interrogation → read shift chain empty	receiver buffer full	send buffer free		Break	parity error	Lost Data
EG Y.3	0	1	1	autom. call	- - - - - - - - - - →		M 24 station disconnected	M 25 power indication	M 23 abandon call	M 22 present next digit	M 21 data line occupied
				modem	- - - - - - - - - - →						
EG Y.4	1	1	1		← interrupt request → shift chain empty	receiver buffer full	send buffer free	M5	M3	M2	M1
EG 0.0.0	0	0	0	← interrupt address →							
AG Y.1	0	0	1	← send buffer →				← digit bits for autom. calling → W 24	W 23	W 22	W 21
AG Y.2	0	1	0	← synchronous character buffer →							
AG Y.3	0	1	1	← changeover timing →			signal negation D1 and D2	← timing rate →			high speed = 1 / slow = 0
AG Y.4	1	0	0	autom. call=1 / modem = 0	I/O test connection D1 to D2	dual stop element	character length 5 to 8 bit		ODD = 1 / EVEN = 0	parity generation	sync = 1 / async = 0
AG Y.5	1	0	1					reset sync FF and receiver	reset interrupt request and buffer	Reset Parity Lost Data Break	Master Reset Sender
AG Y.6	1	1	0						S22 digit present	S21 call request	
								S 4	S 3	S 2	S 1 / Modem
AG 7 (Y0) A9 · 12 = 0	0	0	0	← interrupt address →							
AG 8 (Y.0) A9 · 11 = 0 A12 = 1	0	0	0		← interrupt inhibit → shift chain empty	receiver buffer full	send buffer free	M5	M 3	M 2	M 1
AG 9 (Y.0) A9 · 10 = 0 A11=1,A12=0	0	0	0	← address preselection →							

13.1.1 Description of I/O Assignment

5 input instructions and 9 output instructions are required to control the line.

13.1.1.1 Input Instructions

- EG X.Y.1 — Interrogate the data input buffer (receiver buffer)

  The buffer can be interrogated at any time required, except in the synchronous operating mode and when synchronization has not been completed.

  Interrogation of the buffer triggers the deletion of the "buffer full" message.

  If the buffer is reloaded during the strobe signal EG 1, an incorrect information item can be accepted. This results in the error message "lost data".

- EG X.Y.2 — Interrogate status bits

  Bit 1 — Lost data

  If strobe signal EG 1 is detected before the transfer of a new data item into the input buffer, the error flag is set.

  Bit 2 — Parity error

  If a parity error is detected when serial data is being received a flag is set (pay special attention to parity).

  Bit 3 — Break error message

  This error flag is set if a format fault has been detected in the synchronous operating mode (incorrect sequence: start, 5 to 8 bits, data, stop).

  Lost data, parity error and break can be reset by means of reset 2.

  Bit 4 — Not used

  Bit 5 — Send buffer free

  This bit is "1" when the send buffer is ready to accept new information.

Bit 6 Receiver buffer full

This status bit is equal to "1" if there is a character in the input buffer which has not been processed. This bit is not affected by lost dat.

Bit 7 Send shift chain empty

This status bit is equal to "1" when the send buffer and the shift chain are empty. The message "shift chain empty" only goes to "1" when a transmission has been made i.e. the message "shift chain empty" is not reported immediately after switching on or immediately after master reset sender (AG 5).

A tape card reader message is cleared by master reset sender (AG 5) or by AG 1 (load send buffer).

Bit 8 not used

- EG X.Y.3 Interrogate message signal

This line contains status messages from data communication equipment or from the special sub-assembly for automatic dialling.

Bit 8 Bit 8 = "1": Messages from the AWD
Bit 8 = "0": Messages from data communication equipment

Bit	Data communication equipment	AWD
1	M1 data set ready	M21 data line occupied
2	M2 ready for sending	M22 present next digit
3	M3 calling indicator	M23 abandon call
4	M5 data carrier detector	M25 power indicator
5		M24 distant station connected

- EG X.Y.4 Interrogate interrupt request flags

Bit 1 M1

This bit is set if a change in the interface signal M1 is detected.

Bit 2 M2

This bit is set if a change in the interface signal M2 is detected.

Bit 3 M3

This bit is set if a change in the interface signal M3 from off to on is detected.

Bit 4 M5

This bit is set if a change in the interface signal M5 is detected.

Bit 5 Send buffer free

This bit is set if a character which has been loaded in the send buffer is accepted into the shift again (send buffer free).

Bit 6 Receiver buffer full

This bit is set if there is a valid character in the receiver buffer.

Bit 7 Shift chain empty

This bit is set after a master reset sender (bit 1, AG 5) or NLO when the send buffer has been loaded at least once and the character has been transmitted in its entirety to the data communication equipment.

- EG 0.0.0 Interrogate interrupt

This line is used, after an interrupt from the system, to interrogate the interrupt address of the I/O which requested the interrupt. The interrupt number is in bits 1 to 8.

13.1.1.2 Output Instructions

- AG X.Y.1 Load send buffer

  Bits
  1 to 8 Information to be outputted

  Bits
  1 to 4 Dial bits for automatic selection.

  Dialling information is set out in accordance with the code table below.

Dial bit	4	3	2	1
Switched connection	W24	W23	W22	W21
Dial signal	Bit combination			
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	0	0	0	0
EON	1	1	0	0
SEP	1	1	0	1

  The character EON (end of number) identifies the end of the dial signal sequence and prepares the data communication equipment to receive a signal from the called station (e.g. answering tone) to acknowledge establishment of connection.

  The character SEP (separation) can be inserted in the sequence of dialling digits and enables the automatic dialling equipment to comply with the pauses during the dialling process which are imposed by certain trunk networks.

  The signal status of lines W21 to W24 must not change as long as line S22 "digit present" (AG 6) is switched on.

- AG X.Y.2 Load the sync character buffer

  Bits
  1 to 8 Bits 1 to 8 contain the code of the sync character. The sync character buffer is required in order to compare the sync characters.

- AG X.Y.3 Set the timing rate, timing transition (external, internal) and signal inversion of D1 and D2.

Bits
1 to 4 Output timing rate

Rate (Baud)	Bit 4	Bit 3	Bit 2	Bit 1
9600	0	0	0	0
7200	0	0	1	0
4800	0	0	0	1
3600	0	0	1	1
2400	0	1	0	0
1800	0	1	1	0
1200	0	1	0	1
900	0	1	1	1
600	1	0	0	0
300	1	0	0	1
200	1	0	1	0
150	1	1	0	0
100	1	1	1	0
75	1	1	0	1
50	1	1	1	1

Bit 5 Inversion bit for control signals D1 and D2 of the V24 interface.

Bit 5 = "0": D1 and D2, positive voltage
Bit 5 = "1": D1 and D2, negative voltage

Bit 6 to 7 Timing switching for different operating modes

	Operating mode	Bit 6	Bit 7	Bit 8
1	Internal send and receiver timing	1	0	0
2	External send and receiver timing	0	0	1
3	Internal send timing and external receiver timing	1	1	0
4	External send timing and internal receiver timing	0	1	0

- AG X.Y.4 Load the operating mode register

Bit 1

Bit 1 = "1": Switch the I/O to synchronous operating mode.
Effect: Character format without start or stop element.

Bit 1 = "0": Switch the I/O to asynchronous operating mode.
Effect: Character format in start and stop bit.

Synchronization starts with the start bit.

Bit 2 Parity generation

Bit 2 = "1": Transmitted data is automatically supplemented with on ODD or EVEN parity bit, depending upon how bit 3 is set.

The bit with the highest value character length is replaced by the parity bit which is formed.

Bit 3 ODD/EVEN parity switching

Bit 3 = "1": Transmitted data is supplemented with an ODD parity bit (if Bit 2 = "1") and received data is checked to ensure that it is odd.

Bit 3 = "0": Transmitted data is supplemented with an EVEN parity bit (if Bit 2 = "1") and received data is made EVEN.

Bit 2 is set in EG 2 if the parity of the characters which are received differs from the parity which has been set.

Bit 4 + 5 Definition of character length

Bit 5	Bit 4	Character length (bit)
0	0	5
0	1	6
1	0	7
1	1	8

Note: The parity bit which is generated is included in the length of the character.

Bit 6 Definition of the stop element

Bit 6 = "1": Transmitted data has a double stop element in the asynchronous operating mode.

Bit 7 Switching the I/O to the test operating mode

Bit 3 = "1": Transmitted data D1 is linked internally with the received data.

The voltage level of the line D1 at the modem interface remains negative and the receiver is inhibited for received data from line D2.

Bit 8 Switching to automatic calling and modem operating mode

Bit 8 = "1": Planned significant inputs and outputs are intended for automatic dialling.

Previously set modem conditions are retained.

- AG X.Y.5 Output reset conditions

Bit 1 Reset sender

This resets the sender system before a transmission.

Bit 2 Reset parity, lost data and break

This bit resets the parity error, lost data and break status messages of input line 2.

Bit 3 Reset interrupt request and interrupt buffer

This bit can be used to reset the interrupt request register and the interrupt buffer.

Bit 4 Reset receiver and sync flip-flop

This bit is used to reset the receiver system for the reception of data. Ensure that the operating mode register is not affected by this system reset.

In the synchronous operating mode this reset necessitates character synchronization once more.

- AG X.Y.6 — Set the connected data communication equipment

  This line can be used to drive data communication equipment. This is the case in the modem operating mode with S1 to S4 and for automatic dialling with S21 and S22.

  Control signal S3 is not used in the I/O 1806 at the time of writing.

  Switching from the modem operating mode to automatic dialling and vice versa does not affect previously set control lines. The register is set to "0" by NLO after switching on and the voltage level of the control lines at the V24 interface becomes negative (off state).

- AG X.Y.0 (AG 7) — Corresponds to AG 7 in the I/O assignment when bits 9 to 12 of the output information are "null"-

  Load the 8-bit interrupt register of the 1806.

- AG X.Y.0 (AG 8) — Corresponds to AG 8 in the I/O assignment when bits 9 to 11 = "0" and bit 12 = "1" in the output information.

  Set or reset the interrupt inhibit bits.

  Interrupt inhibit = "1": The corresponding channel is inhibited.

  Interrupt inhibit = "0": The corresponding channel is enabled.

  All channels are inhibited after switching on.

- AG X.Y.0 (AG 9) — Corresponds to AG 9 in the I/O assignment when bits 9 and 10 = "0", bit 11 = "1" and bit 12 = "0".

  An address preselection is performed.

  The number of the I/O 1806 to be preselected is in bits 1 to 8. Preselection remains valid until the next address preselection.

13.2 Interrupt Release

The communication of the I/O is interrupt-controlled. See interrupt release by means of interrupt request bits on EG 3.

13.3 Addressing

The I/O is addressed by preselection (output instruction AG 9) and by means of the PSP address.

Preselection is necessary since it is possible that there can be several I/O cards in the system and these I/O cards can be addressed via the same PSP address (1.F.0 at the time of writing).

Line	Address	Preselection
1. Trunk line	1.F.0	0.0
2. Trunk line	1.F.0	0.1
3. Trunk line	1.F.0	0.2
4. Trunk line	1.F.0	0.3
5. Trunk line	1.F.0	0.4
6. Trunk line	1.F.0	0.5

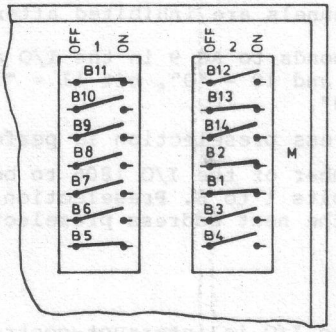
13.4 Interface Wiring

Various V24 interface circuits (coding switches) can be used so that the I/O can be connected to various data communication equipment.

The V24 interface can be modified by changing the switch positions of the two built-in 7-pin AMP switches in order to drive various data communication equipment.

The switches are located on the component side of the I/O at IC positions M1 and M2.

Coding switches (DIL switch)



Interface signal		Example of application	Switch
M1	From the data transmission unit e.g. modem	normal	B 6
	set at +12V	connected to node 0513	B 5
M2	From the data transmission unit	normal	B 8
	set at +12V	connected to node 0513	B 7
	routed to S2	connected to node 0513	B 2
M3	From the data transmission unit	normal	B 10
	set at +12V		B 9
	set at - 5V	for installations without remote connection (e.g.900M1)	B 11
M5	From the data transmission unit	normal	B 13
	set at +12V	for direct connection where required	B 12
S2	Controlled by operating program	normal	B 1
	set at +12V	full duplex data transmission unit and line wiring	B 14
	Routed to M2	e.g. connected to node 0513	B 2
S4	Controlled by operating program		B 4
	set at +12V	high speed data transfer rate with D 1200 S = 1200 bit/s.	B 3

13.5 V24 Interface Wiring with SC and SD Connector

(In accordance with DIN standard 66020 and CCITT standard)

If the voltage level of a signal on a data line with respect to line E2 (signal ground) or the voltage level of a signal on a select line with respect to line E22 (ground signal) differs from 0 volt and is

a) negative, the signal state is "1",
b) positive, the signal state is "0".

The signal state is indeterminate in the transitional range between +3V to -3V.

If the voltage level of a signal on a control line or on a message line differs by more than 5 volts with respect to the relevant "signal ground" line, and is

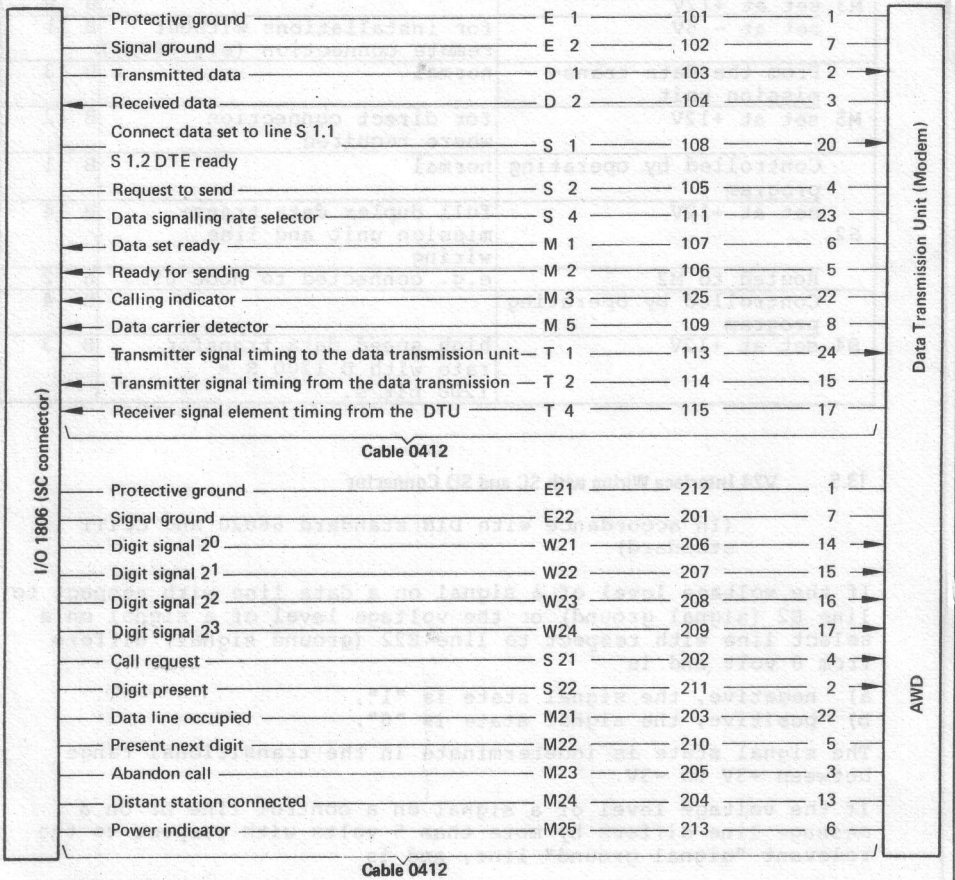
a) negative, the line is quiescent,
b) positive, the line is in the on condition.

The signal state is indeterminate in the transitional range between +3V to -3V.

If the voltage level of a signal on a timing line differs by more than 3 volts with respect to line E2 (signal ground) and is

a) negative, the line is quiescent,
b) positive, the line is in the on condition.

- Summary of Interface Lines



- Example of interface wiring (DIL switch)

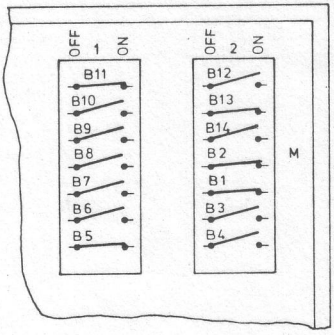
Data communication with a long distance line is via node 0513.

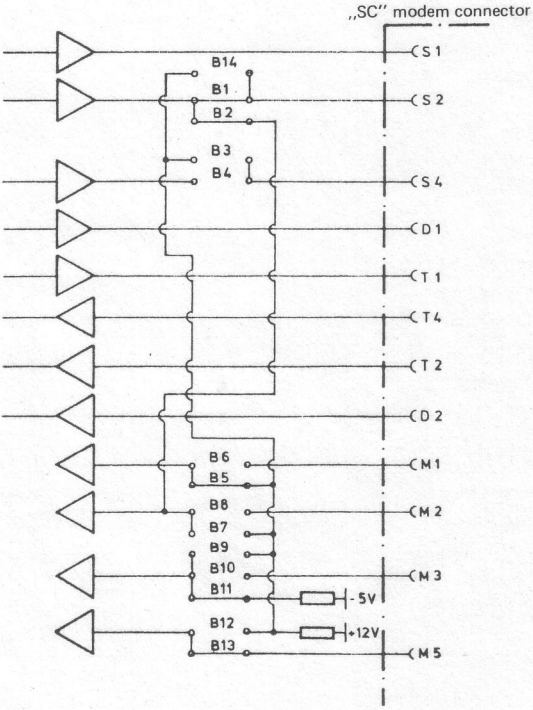
S2 (Request to send) is taken through and looped back to M2 (ready for sending) (B1, B2).

M1 (Data set ready) is set at +12V (b5).

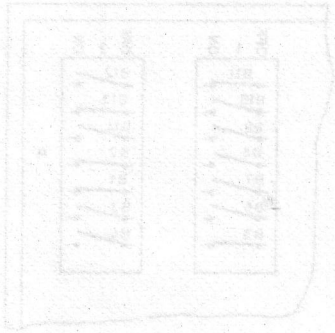
M3 (Calling indicator for remote switching) is set at -5V (B11).

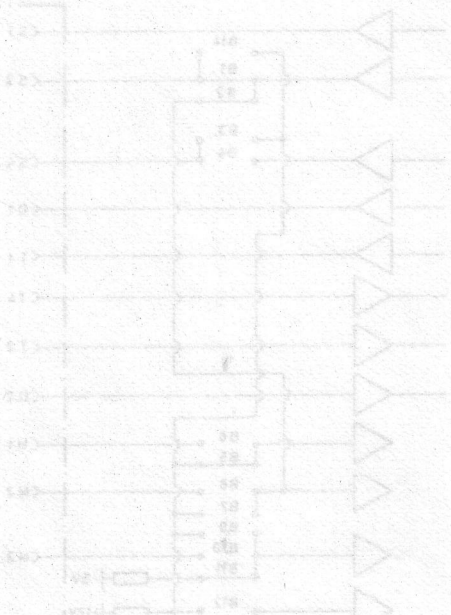
M5 (Data carrier detector) is taken through (B13).





For notes





14 DTEA 1813

The I/O is used to control display 0608.01 and keyboard 0687.00 or 0687.02 via the PSP.

14.1 I/O Assignment

I/O Instr. \ Bit	Information cycle 8	7	6	5	4	3	2	1	I/O device	
EG 0.0	0	0	← interrupt number →					0	T	input interrupt number
EG Y.0	0	0	← interrupt number →					0	T	input interrupt number
EG Y.1	← char. code →								T	input information
EG Y.2	INT	0	0	0	0	LD	PFS	Lo	T	status input
EG Y.3	0	0	0	ETB4	ETB3	ETB2	ETB1	ETB0	T	input individual characters
EG Y.4	x	x	x	x	0	0	PFS	Lo	D	status input
EG Y.7	← char. code →								D	input picture refresh memory
AG Y.1	240 ms adder	red lamp	yellow lamp	LED 5	LED 4	LED 3	LED 2	LED 1	A	output indicator
AG Y.2	INT KSP	x	x	x	x	x	MLO	LOB	T	status output
AG Y.3	← free →								T	
AG Y.4	x	SU	CI	CS	x	BS	MLO	LOB	D	output operational status
AG Y.5	x	x	x	x	← Cursor Y →				D	output Y cursor
AG Y.6	x	← Cursor X →							D	output X cursor
AG Y.7	← char. code →								D	output picture refresh memory

A – Pointer indicator
D – Display
T – Keyboard

14.1.1 Description of I/O Assignment

Seven input instructions and seven output instructions are required to control the display and the keyboard.

14.1.1.1 Input Instructions

- EG 0.0 — Interrogate interrupt number.
- EG Y.0 — Interrogate content of interrupt register.
- EG Y.1 — Interrogate keyboard code.
- EG Y.2 — Interrogate keyboard status bits.

Bit 1 — LO, "reset" flag

Bit 1 = "1": reset as result of an initial reset signal (output LOB on AG Y.2).

This bit is reset by outputting MLO (bit 2) on AG Y.2.

Bit 2 — PFS, parity error flag

Bit 2 = "1": A parity error has occurred in the PSP during the information cycle of the last output instruction.

This flag is reset by outputting MLO (bit 2) on AG Y.2.

Bit 3 — LD, lost data

Bit 3 = "1": Lost data, i.e. a new character has been entered from the keyboard and the previous character has not been picked up.

LD is reset by outputting MLO (bit 2) on AG Y.2.

Bit 4 to 7 — Not used

Bit 8 — INT, interrupt flag

Bit 8 is set when a new character from the keyboard is made available. An interrupt is released if the interrupt condition is enabled. INT is reset by means of EG Y.1.

- EG Y.3 — Input individual characters

  Bit 1 to 5 — These 5 individual bits correspond to the 5 key-operated switches of the keyboard (They are not used on the 8870).

- EG Y.4 — Interrogate display status bits

  Bit 1 — LO, delete flag

  This flag is set when an initial reset has been performed by outputting LOB on AG Y.4. This flag is reset by outputting MLO (bit 2) on AG Y.4.

  Bit 2 — PFS, parity error flag

  A parity error has occurred in the PSP during the information cycle of the last output instruction.

  This flag is reset by outputting MLO (bit 2) on AG Y.4.

  Bit 3 to 8 — Not used

- EG Y.7 — Input picture refresh memory

  Interrogate picture refresh memory.

14.1.1.2 Output Instructions

- AG Y.1 — Output indicator

  Information for the keyboard lamps and the keyboard LED's is outputted.

Output information (Bit)	LED
1	1 (top LED)
2	2
3	3
4	4
5	5 (bottom LED)
6	yellow lamp
7	red lamp
8	adder (240 ms)

- AG Y.2 Output status

  Bit 1 LOB

  The DTEA is reset by outputting LOB. When this occurs LO is set in status line EG Y.2.

  Bit 2 MLO

  The keyboard flag LO PFS on the status line EG Y.2 are reset by outputting MLO.

  Bit 3 to 7 Not used

  Bit 8 INT-KSP

  Interrupt release by means of the keyboard is inhibited by outputting bit 8 = "1".

  Bit 8 = "0": cancel interrupt inhibit

  The flag INT (bit 8 on EG Y.2) is not affected when an interrupt is inhibites or reset.

- AG Y.4 Output operating status

  The operating mode of the display is outputted.

  Bit 1 LOB

  The DTEA is reset when this bit is outputted. When this occurs bit 1 (LO) is set on line EG Y.4.

  Bit 2 MLO

  The flags LO and PFS on EG Y.4 are reset when MLO is outputted.

  Bit 3 BS

  Bit 3 = "1": The monitor is enabled for visual display.

  Bit 3 = "0": The monitor is inhibited for visual display.

Bit 6 CI

Bit 6 = "1": The monitor is enabled in the 960-character operating mode.

Bit 6 = "0": The monitor is enabled in the 480-character operating mode.

Bit 7 SU

Bit 7 = "1": Page 1 is displayed with 480 characters.

Bit 7 = "0": Page 2 is displayed with 480 characters.

Bit 8 Not used

- AG Y.5 Output Y cursor

  Bits 1 to 4 These bits indicate the position of the cursor on the Y axis.

- AG Y.6 Output X cursor

  Bits 1 to 7 These bits indicate the position of the cursor on the X axis.

- AG Y.7 Output picture refresh memory

  This instruction loads the picture refresh memory.

14.2 Interrupt Release

The DTEA can release interrupts. An interrupt can be released by depressing a key on the keyboard provided that the interrupt enable (bit 8 = "0") has been outputted on AG Y.2.

Interrupt release is not used with the 8870. The DTEA is controlled via the clock interrupt.

14.3 Addressing

Addressing is via the coupling unit connected to the PSP interface.

Address structure

8	4	2	1	8	4	2	1	Value
8	7	6	5	4	3	2	1	Bit
INF 7	INF 6	INF 5	INF 4	INF 3	INF 2	INF 1	INF 0	Information line
← device address →					← I/O line →			

The addresses used at time of writing:

Address (with respect to EG 0)	Work station	PSP bus
3.1.0	1.	1
3.1.8	2.	1
3.2.0	3.	1
3.2.8	4.	1
3.3.0	5.	1
3.3.8	6.	1
3.4.0	7.	1
3.4.8	8.	1
3.5.0	9.	1
7.1.0	1.	2
7.1.8	2.	2
7.2.0	3.	2
7.2.8	4.	2
7.3.0	5.	2
7.3.8	6.	2
7.4.0	7.	2
7.4.8	8.	2

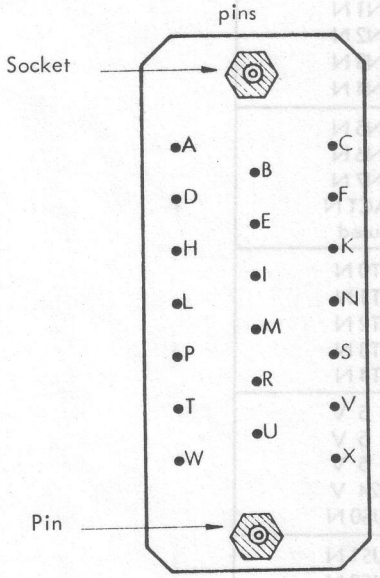
There can only be 8 work stations on PSP bus 2 because the console must be on PSP bus 1.

14.4 Wiring Diagrams and Connector Assignment

33-pin SEL connector (BB)
PSP interface

1	GND
2	IF0N
3	IF1N
4	IF2N
5	GND
6	IF3N
7	IF4N
8	IF5N
9	GND
10	IF6N
11	IF7N
12	PARN
13	GND
14	AGN
15	unused
16	STADN
17	GND
18	STIN
19	QUITTN
20	INTN
21	GND
22	INSAN
23	INSEN
24	NEN
25	LON
26	Uss
27	+ 5 V
28	+ 5 V
29	- 12 V
30	GND
31	GND
32	+ 24 V
33	+ 24 V

Device connector assignment



Contact	Signal
A	
B	
C	A3N
D	A4N
E	GND
F	A5N
H	A6N
I	A7N
K	
L	
M	
N	
P	
R	GND
S	
T	
U	
V	
W	
X	

Contacts are shown as seen on the pin wiring side.
20-pin Winchester connector SRE 20 PD NSS H 13

Contact arrangement of the 37-pin Cannon socket connector "D"

1	EIN0 N
2	EIN1 N
3	EIN2 N
4	EIN3 N
5	EIN4 N
6	EIN5 N
7	EIN6 N
8	EIN7 N
9	KACT N
10	unused
11	EBT0 N
12	EBT1 N
13	EBT2 N
14	EBT3 N
15	EBT4 N
16	+ 5 V
17	+ 5 V
18	+ 5 V
19	+ 24 V
20	AUS0 N
21	AUS1 N
22	AUS2 N
23	AUS3 N
24	AUS4 N
25	AUS5 N
26	AUS6 N
27	AUS7 N
28	WTAUS N
29	LOT N
30	NE N
31	unused
32	unused
33	unused
34	GND
35	GND
36	GND
37	GND

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